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U.S. DEPARTMENT OF COMMERCE / National Bureau of Standards

*Semiconductor Measurement Technology:*

**Microelectronic  
Test Pattern NBS-4**

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# *Semiconductor Measurement Technology:*

## **Microelectronic Test Pattern NBS-4**

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W. Robert Thurber and  
Martin G. Buehler

Electronic Technology Division  
Institute for Applied Technology  
National Bureau of Standards  
Washington, D.C. 20234

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and  
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## PREFACE

The work was conducted as part of the Semiconductor Technology Program at the National Bureau of Standards. Portions of this work were supported by the Defense Advanced Research Projects Agency (Order No. 2397) and the NBS.

In the semiconductor industry it is common practice to design photomasks in English units. The photomasks used in this study were laid out in English units. The equivalent metric unit is given in parentheses; in some cases the equivalent is rounded off to an appropriate number of significant figures.

The authors wish to thank several members of the Electronic Technology Division for their assistance. Y. M. Liu developed the wafer fabrication processes, W. A. Cullins prepared most of the drawings, Cindy Cannon photographed the wafers and masks, and Jane Walters typed the manuscript.



by

W. Robert Thurber and Martin G. Buehler

*Abstract:* Microelectronic test pattern NBS-4 is a revision of test pattern NBS-3 which was designed primarily for evaluation of the resistivity-dopant density relationship in silicon. Major changes include the addition of optional BASE-CONTACT and GATE masks and the incorporation of several new structures, some useful for the resistivity-dopant density work, and others, mostly sheet resistors, included for evaluation of new designs.

The NBS-4 pattern contains 38 test structures such as planar four-probe resistors, sheet resistors, MOS capacitors,  $p$ - $n$  junctions, bipolar and MOS transistors, Hall effect device, and process control structures. The overall pattern is a square 200 mil (5.08 mm) on a side and is divided into four quadrants which are separated by scribe lines. A detailed layout of each structure is presented including both a top view and a cross sectional view. Photomicrographs of each quadrant and the quadrants of the six masks used in the fabrication of the pattern are shown in an appendix.

*Key Words:* Dopant density; microelectronics; MOS capacitors;  $n$ - $p$ - $n$  transistor fabrication;  $p$ - $n$  junctions; resistivity; semiconductor electronics; sheet resistors; silicon; test pattern; test structures.

## 1. INTRODUCTION

The purpose of this report is to describe the microelectronic test structures found on test pattern NBS-4. This is accomplished primarily by drawings of the structures, supplemented by photomicrographs of the masks and fabricated wafers. Test pattern NBS-4 is a revision of test pattern NBS-3 [1] which was designed for study of the resistivity-dopant density relationship in silicon. Significant changes include the addition of optional BASE-CONTACT and GATE masks and the incorporation of new structures for the resistivity-dopant density work and for the measurement of sheet resistance. The pattern is composed of an array of 38 test structures, such as planar four-probe resistors, sheet resistors, MOS capacitors,  $p$ - $n$  junctions, bipolar and MOS transistors, Hall effect device, and process control structures, which for the most part are adaptations of commonly used configurations. Table 1 gives a list of the test structures, their purpose, and one or more references with details on their use. A majority of the structures are the same, or very similar, to ones on test pattern NBS-3, and the publication [1] on that pattern includes discussion of each structure, equations for calculation of the quantities determined by each, and additional references.

The devices specifically designed for the resistivity-dopant density evaluation are indicated by an asterisk in table 1. The square array four-probe resistor [2] has proven to be the best structure for resistivity measurements, and four structures of the same basic design, differing only in the size of the collector pipes, were added as part of NBS-4. Two new MOS capacitor structures were added for dopant density measurements. These devices are designed for steady-state, deep-depletion, capacitance-voltage measurements. Bulk dopant density values can be obtained from the following structures: MOS capacitors (4.2, 4.3, and 4.8), base-collector diode (4.10), MOSFET

Table 1 - Planar Test Structures on Test Pattern NBS-4

Page	Structure Number	Test Structure <sup>a</sup>	Purpose	References
12	4.1	*Collector resistor (pipes 0.20 mil on a side)	Resistivity	1,2
15	4.2	*MOS capacitor over collector (base DGR)	Dopant density	4
16	4.3	*MOS capacitor over collector (emitter DGR)	Dopant density	4
23,24	4.4	Alignment markers	Mask alignment	
12	4.5	*Collector resistor (pipes 0.30 mil on a side)	Resistivity	1,2
24	4.6	Logo	Identification	
12	4.7	*Collector resistor (pipes 0.40 mil on a side)	Resistivity	1,2
17	4.8	*MOS capacitor over collector (FP, CS)	Dopant density, $V_{fb}$	1,5
12	4.9	*Collector resistor (pipes 0.50 mil on a side)	Resistivity	1,2
19	4.10	*Base-collector diode (FP, CS)	Dopant density	1,6
7	4.11	Base sheet resistor (VDP, FP, CS)	Sheet resistance	1,3
18	4.12	MOS capacitor over base	Surface dopant density	1
20	4.13	Bipolar transistor	Proper fabrication	1,7
20	4.14	Base-collector diode (FP, CS)	Dopant density	1,8
21	4.15	*MOSFET (circular, W/L = 18.2)	Dopant density	1,9
22	4.16	MOSFET (rectangular, W/L = 4)	Proper fabrication	1
12	4.17	*Collector resistor (pipes 0.25 mil on a side)	Resistivity	1,2
14	4.18	Collector spreading resistor	Back-side resistance	1,10
11	4.19	Metal sheet resistor (Greek cross)	Sheet resistance	1
9	4.20	Base-under-emitter sheet resistor (Greek cross)	Sheet resistance	7,11
10	4.21	Base-contact sheet resistor (Greek cross)	Sheet resistance	12
6	4.22	Base sheet resistor (narrow Greek cross)	Sheet resistance	3,12
9	4.23	Base sheet resistor (B, W/L = 0.25)	Sheet resistance	7,13
6	4.24	Base sheet resistor (Greek cross)	Sheet resistance	2,12
6	4.25	Base sheet resistor (Greek cross, tab contacts)	Sheet resistance	2,12
6	4.26	Base sheet resistor (offset quadrate cross)	Sheet resistance	2,12
11	4.27	Metal-to-emitter contact resistor	Contact resistance	1
10	4.28	Emitter sheet resistor (offset quadrate cross)	Sheet resistance	1,12
11	4.29	Metal-to-base contact resistor	Contact resistance	1
17	4.30	MOS capacitor over collector (square)	Measurement limitations	1
13	4.31	*Hall effect device (VDP)	Carrier density	1,14
10	4.32	Emitter sheet resistor (B, W/L = 0.25)	Sheet resistance	1
9	4.33	Base sheet resistor (B, W/L = 0.25)	Sheet resistance	1,13
25	4.34	Surface profilometer structure	Process control	1
8	4.35	Incremental base sheet resistor (VDP)	Dopant profile	1,3
26	4.36	Etch-control structures <sup>c</sup>	Process control	1
26	4.37	Resolution structures <sup>c</sup>	Process control	1
13	4.38	Metal step-coverage resistor	Metal continuity	1

\* = structures designed for resistivity-dopant density evaluation.

<sup>a</sup>B = bridge; CS = channel stop; DGR = diffused guard ring; FP = field plate; L = length along current path; VDP = van der Pauw; W = width of current path.

<sup>b</sup> $V_{fb}$  = flat band voltage.

<sup>c</sup>B = BASE mask; BC = BASE-CONTACT mask; C = CONTACT mask; E = EMITTER mask; G = GATE mask; M = METAL mask.



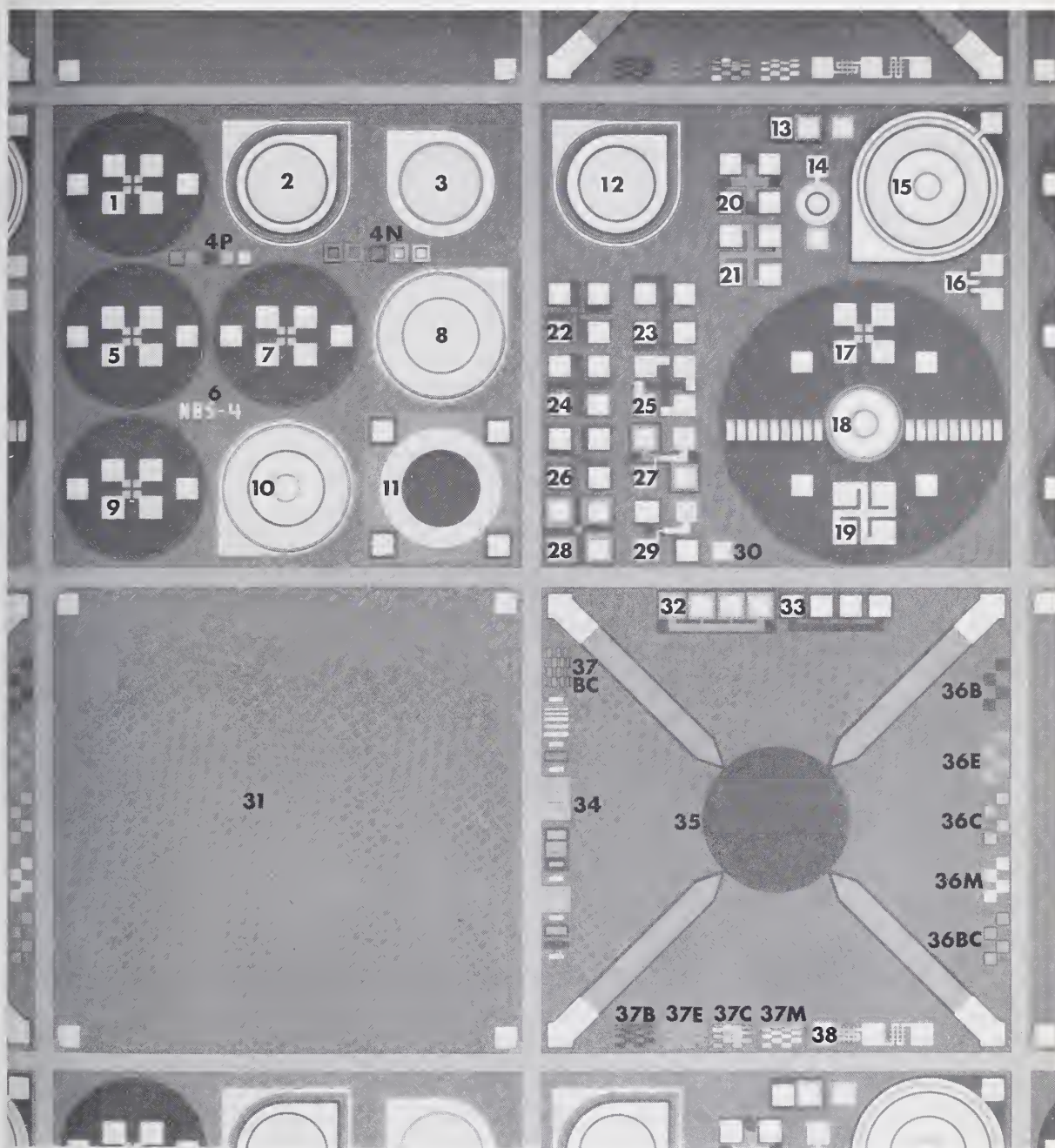


Figure 1. Test pattern NBS-4 fabricated with BASE (B), EMITTER (E), BASE-CONTACT (BC), CONTACT (C), and METAL (M) masks. The length of the pattern along one side is 200 mil (5.08 mm).

(4.15), and Hall effect device (4.31). Bulk resistivity values can be found from the square array four-probe collector resistors (4.1, 4.5, 4.7, 4.9, and 4.17) and the Hall effect device (4.31). It should be noted that the collector Hall effect device (4.31) is functional only after it has been scribed from the wafer and the back-side metal removed. To accommodate this structure, the scribe grid was omitted from the BASE and EMITTER masks and included on only the CONTACT and GATE masks.

The new pattern also contains eight base sheet resistors, four of which were not included on test pattern NBS-3. Comparative measurements have been made on the six van der Pauw base sheet resistors [3]. The base-under-emitter sheet resistor (4.20) is a new structure on the pattern. The metal sheet resistor (4.19) is of somewhat different design than that on test pattern NBS-3 to avoid the problem of burnout due to high current density in narrow connecting arms. The incremental base sheet resistor (4.35) was modified slightly from the one on test pattern NBS-3. The width of the arms near the body was increased to minimize arm resistance which is especially important as the structure is thinned by repeated layer removal. The addition of the base-contact diffusion in the arms further reduces the resistance. Also, the metal contact pads were enlarged to allow multiple wire bonds. Many of the remaining test structures are in support of the primary devices. They were included to provide tests which can assure that proper fabrication steps have been followed and aid in diagnosing problems.

A photomicrograph of test pattern NBS-4 is shown in figure 1. The overall pattern is 200 mils (5.08 mm) on a side and is divided into four quadrants. Enlarged views of each quadrant of the fabricated test pattern and the six masks are shown in the Appendix. The masks are: BASE, BASE-CONTACT, EMITTER, GATE, CONTACT, and METAL. The BASE and BASE-CONTACT masks delineate regions to be diffused with a conductivity type opposite from the collector substrate and the EMITTER mask delineates regions to be diffused with a conductivity type the same as the collector substrate. Emitter-diffused regions are more heavily doped than the collector. The BASE-CONTACT mask is designed to delineate heavily doped diffused regions where electrical contacts are made to base-diffused regions. It is intended for use in the processing of  $p$ -type wafers where low resistance contacts to  $n$ -type base regions are a problem. With respect to the placement of the alignment markers, the base-contact diffusion was designed to follow the base diffusion. However, the diffusions do not have to be done in this order and in the processing sequence used for the resistivity-dopant density study the base-contact diffusion was made following the emitter diffusion so that the surface dopant density of the base-contact regions was not reduced by any subsequent high-temperature processing steps. The BASE-CONTACT mask is generally not used for  $n$ -type wafers as aluminum makes good electrical contact to the typical  $p$ -type base diffusion. The GATE mask is used whenever a thin, high quality oxide is needed for the MOS devices. During this step, which follows the diffusions, the previous oxide is removed in the areas delineated by the GATE mask and new oxide is grown.



## 2. TEST STRUCTURES

This section discusses the notation used on the drawings of the test structures which follow in sections 3 through 7. The structures are grouped in five major categories: resistors, MOS capacitors, diodes, transistors, and miscellaneous. The new structures on the pattern were designed using the same design rules as for test pattern NBS-3 [1].

In the following sections both a detailed top view layout and cross sectional view of each test structure are given. Figure 2 illustrates the scheme used. In the top views and in the horizontal direction for cross sectional views, the distance between grid lines represents 0.50 mil (12.7  $\mu\text{m}$ ). In the cross sectional views, metal regions are black and oxide regions are dotted. All oxide areas are shown with a thickness of one unit above the silicon surface with the exception of gate oxide regions which are only a half unit thick. In top views the gate oxide regions are denoted by dashed lines as there is frequently not a line in the cross sectional view to indicate the boundary of the gate oxide. Regions with a base diffusion are clear and indicated by a solid line two units below the silicon surface. Regions with an emitter diffusion are clear and indicated by a solid line one unit below the silicon surface. Regions with a base-contact diffusion are clear and indicated by a solid line one-half unit below the silicon surface. (In these views a *unit* is the distance between adjacent grid lines. Also the silicon surface is assumed to be flat for the sake of simplicity; the incorporation of silicon into the oxide during thermal oxidation has been ignored.)

The following notation is used to define metal contact pads on the top view of the drawings:

B = base contact	G = gate contact	$I_1, I_2$ = current contacts
C = collector contact	S = source contact	$V_1, V_2$ = voltage contacts
E = emitter contact	D = drain contact	

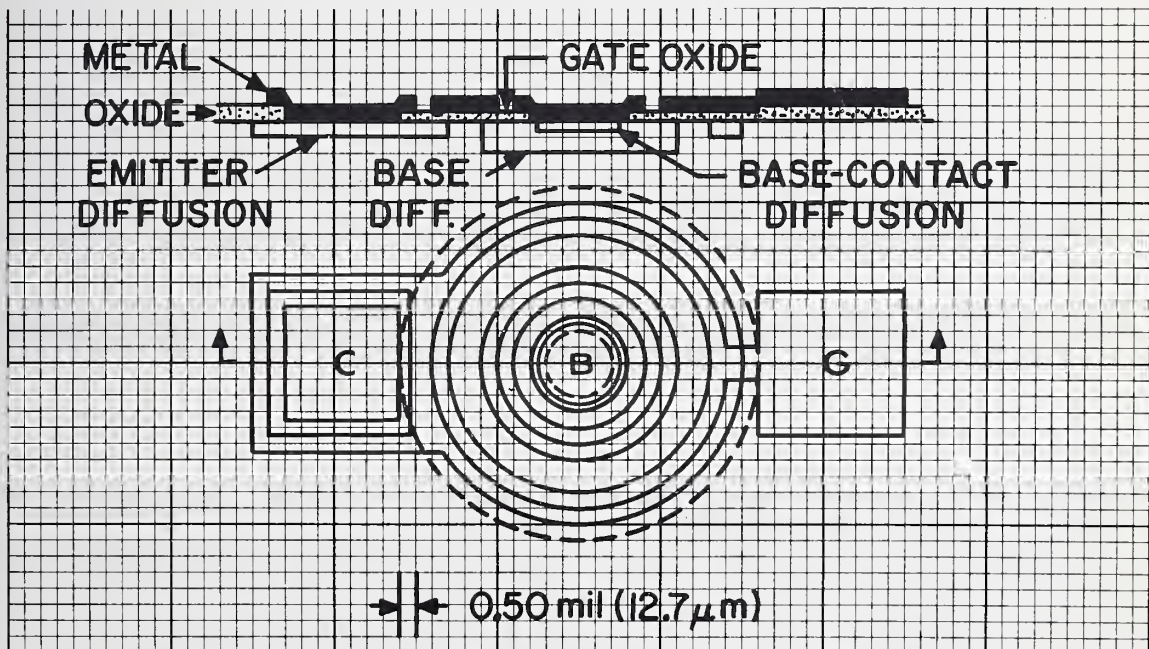
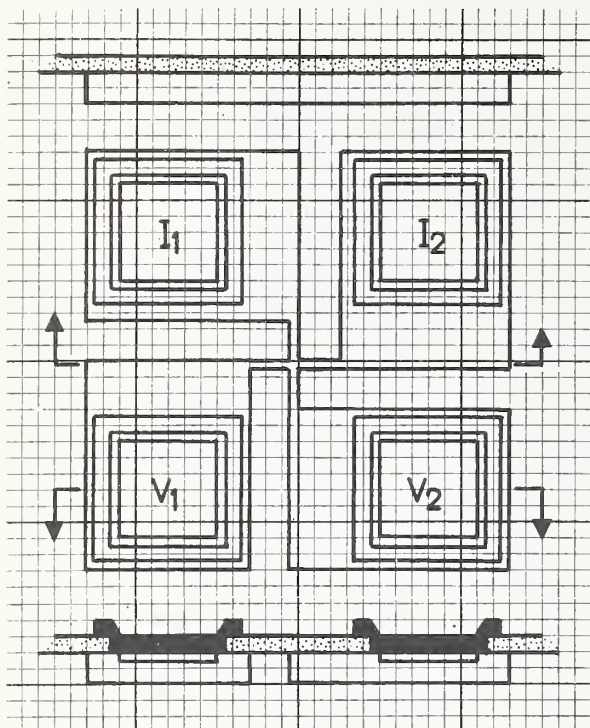


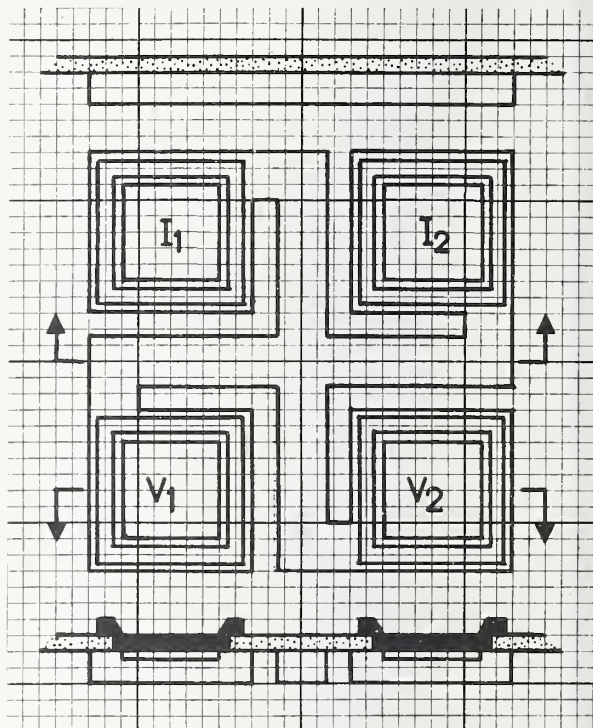
Figure 2. An illustration of the notation used in views of a test structure. The emitter diffusion is used for emitter regions of a bipolar transistor, channel stop (CS) regions, and low-resistance contacts to the collector. The base diffusion provides both bipolar transistor base regions and MOS transistor source-drain regions.

### 3. RESISTORS

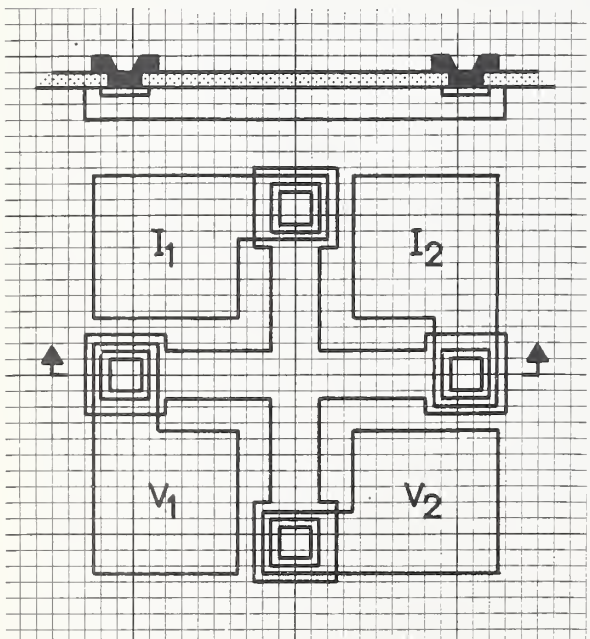
3.1 Base Sheet Resistor  
(Greek Cross)  
Structure 4.22



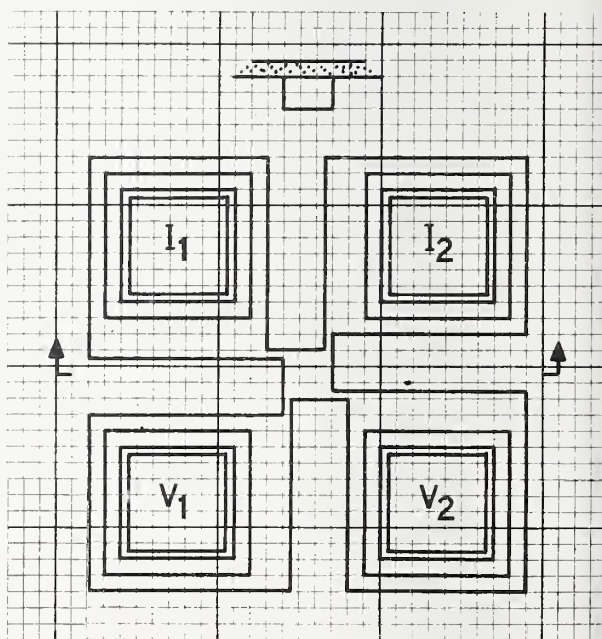
3.2 Base Sheet Resistor  
(Greek Cross)  
Structure 4.24



3.3 Base Sheet Resistor  
(Greek Cross)  
Structure 4.25

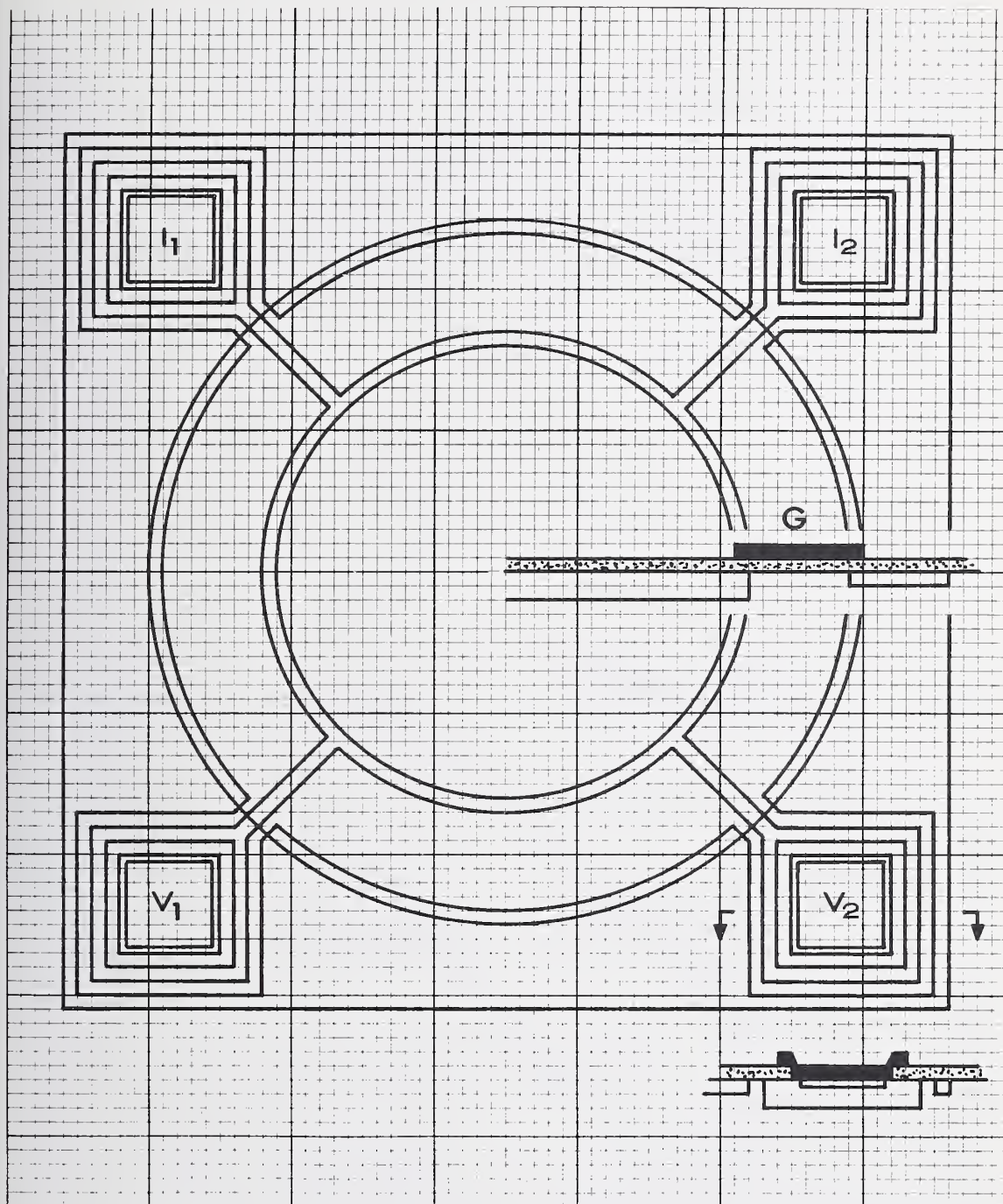


3.4 Base Sheet Resistor  
(Offset Quadrate Cross)  
Structure 4.26

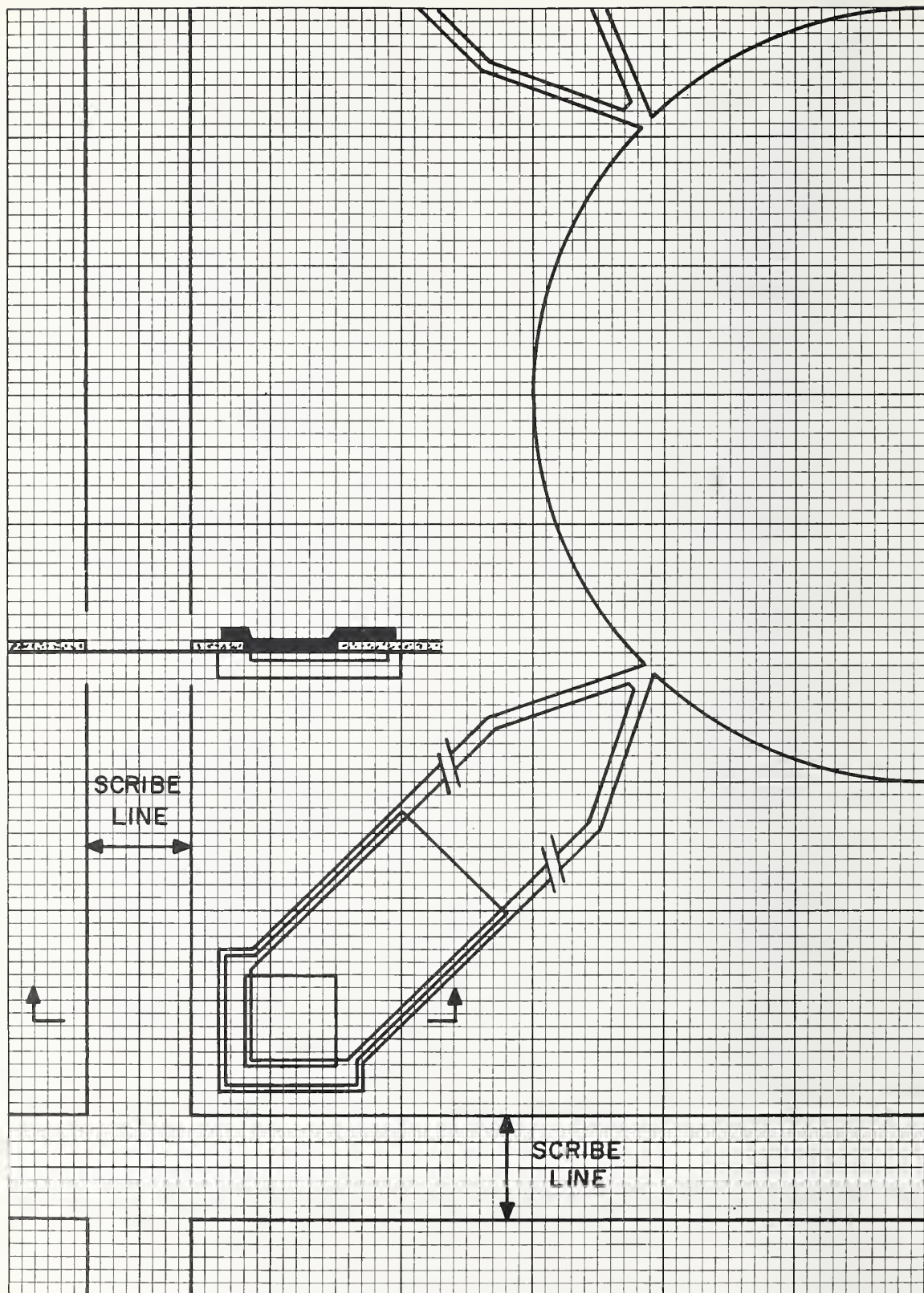




3.5 Base Sheet Resistor (van der Pauw, field plate, channel stop)  
Structure 4.11

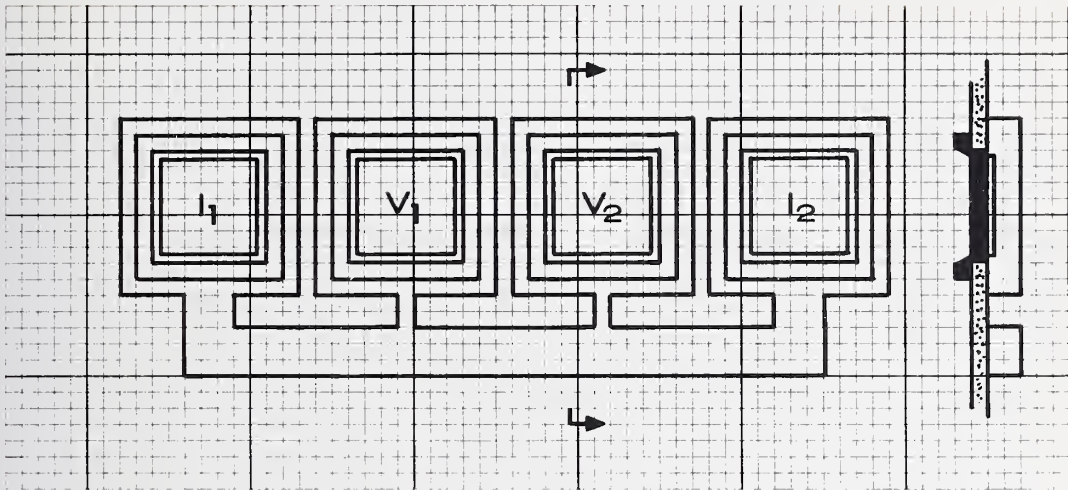


3.6 Incremental Base Sheet Resistor (van der Pauw)  
Structure 4.35

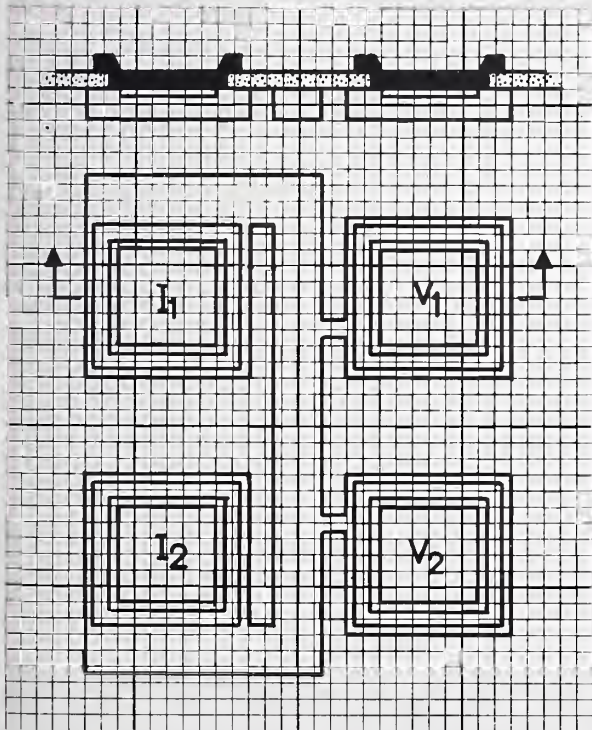




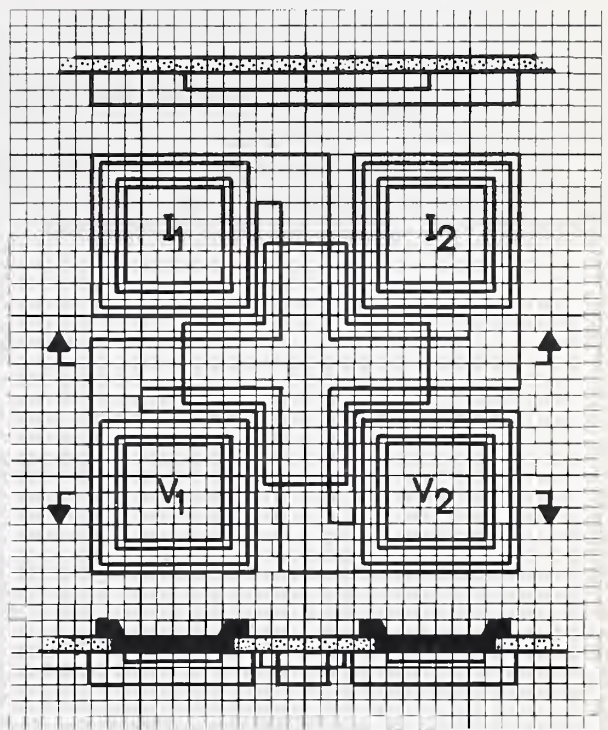
3.7 Base Sheet Resistor (Bridge)  
Structure 4.33



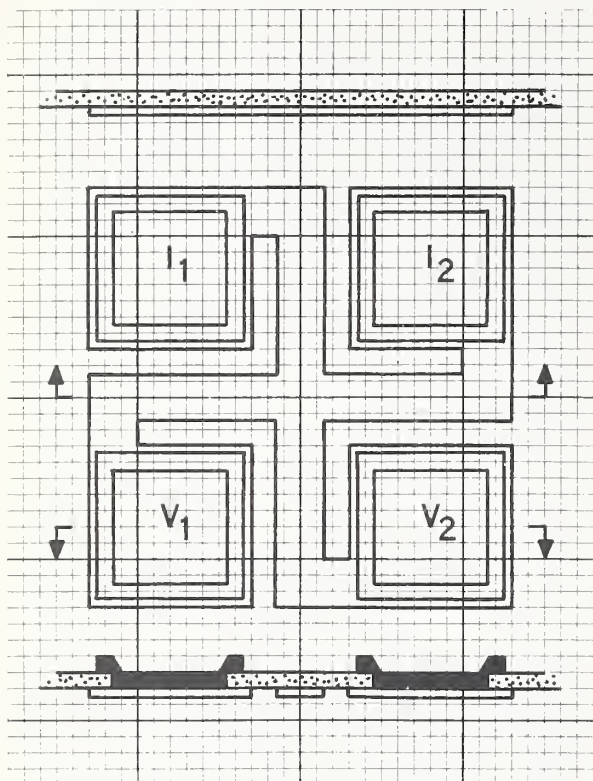
3.8 Base Sheet Resistor  
(Bridge)  
Structure 4.23



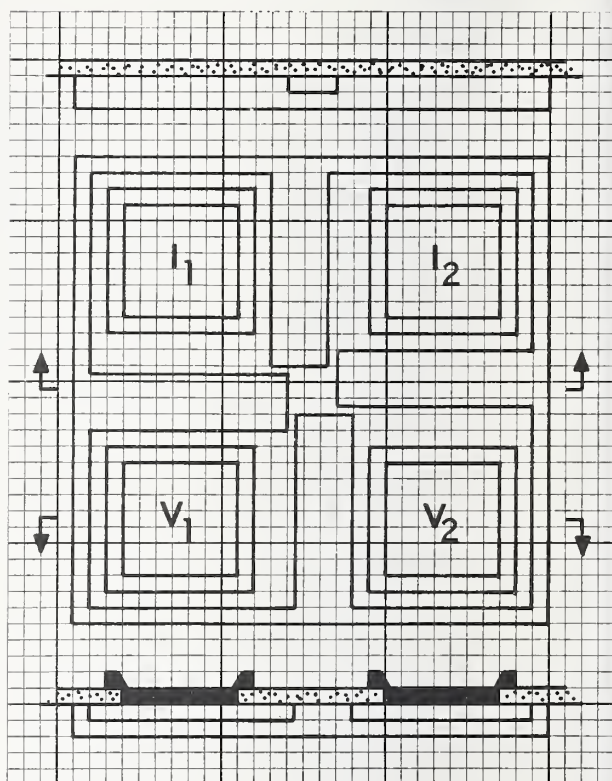
3.9 Base-under-Emitter Sheet Resistor  
(Greek Cross)  
Structure 4.20



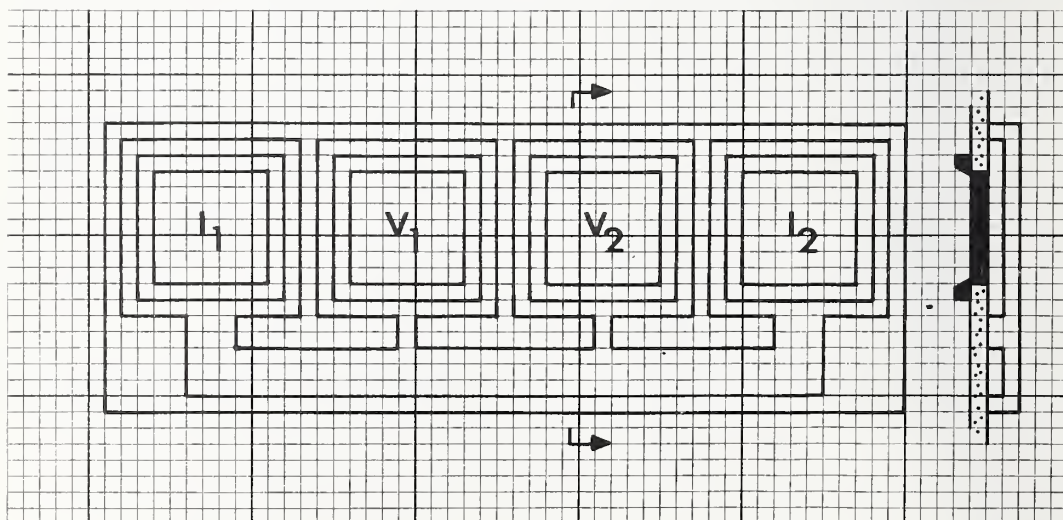
3.10 Base-Contact Sheet Resistor  
(Greek Cross)  
Structure 4.21



3.11 Emitter Sheet Resistor  
(Offset Quadrate Cross)  
Structure 4.28

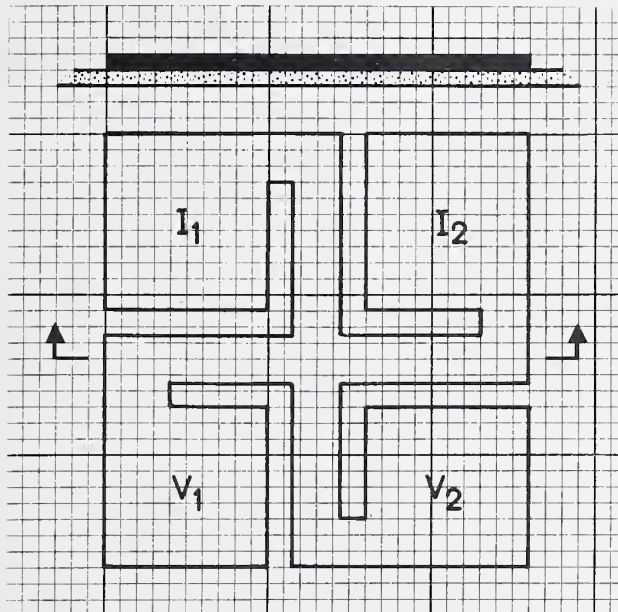


3.12 Emitter Sheet Resistor (Bridge)  
Structure 4.32

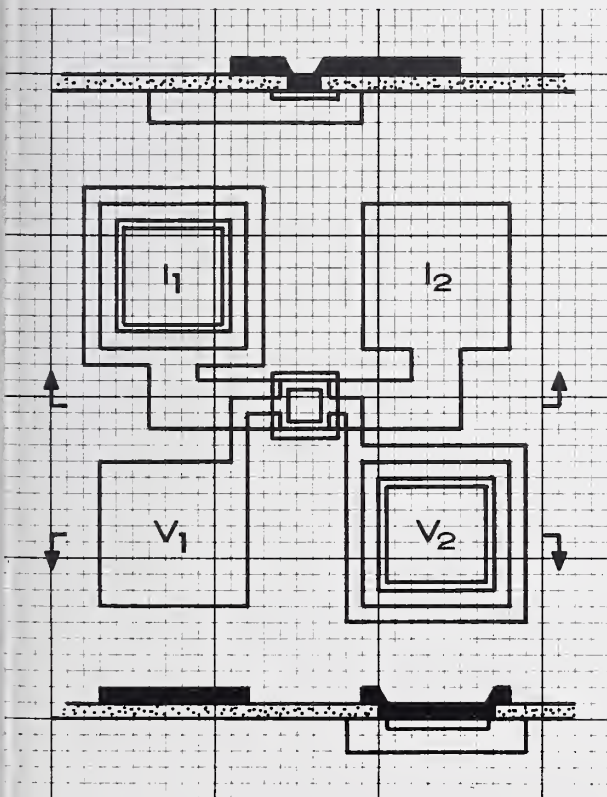




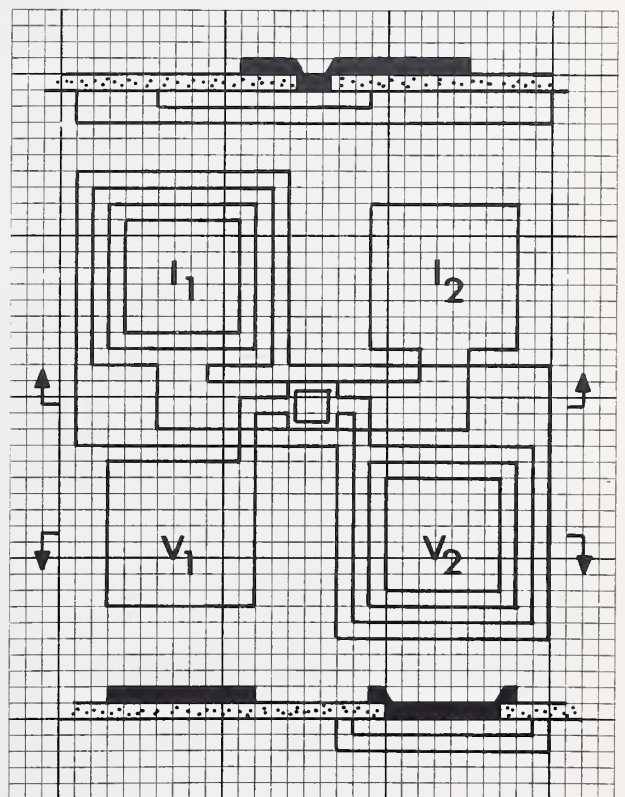
3.13 Metal Sheet Resistor  
(Greek Cross)  
Structure 4.19



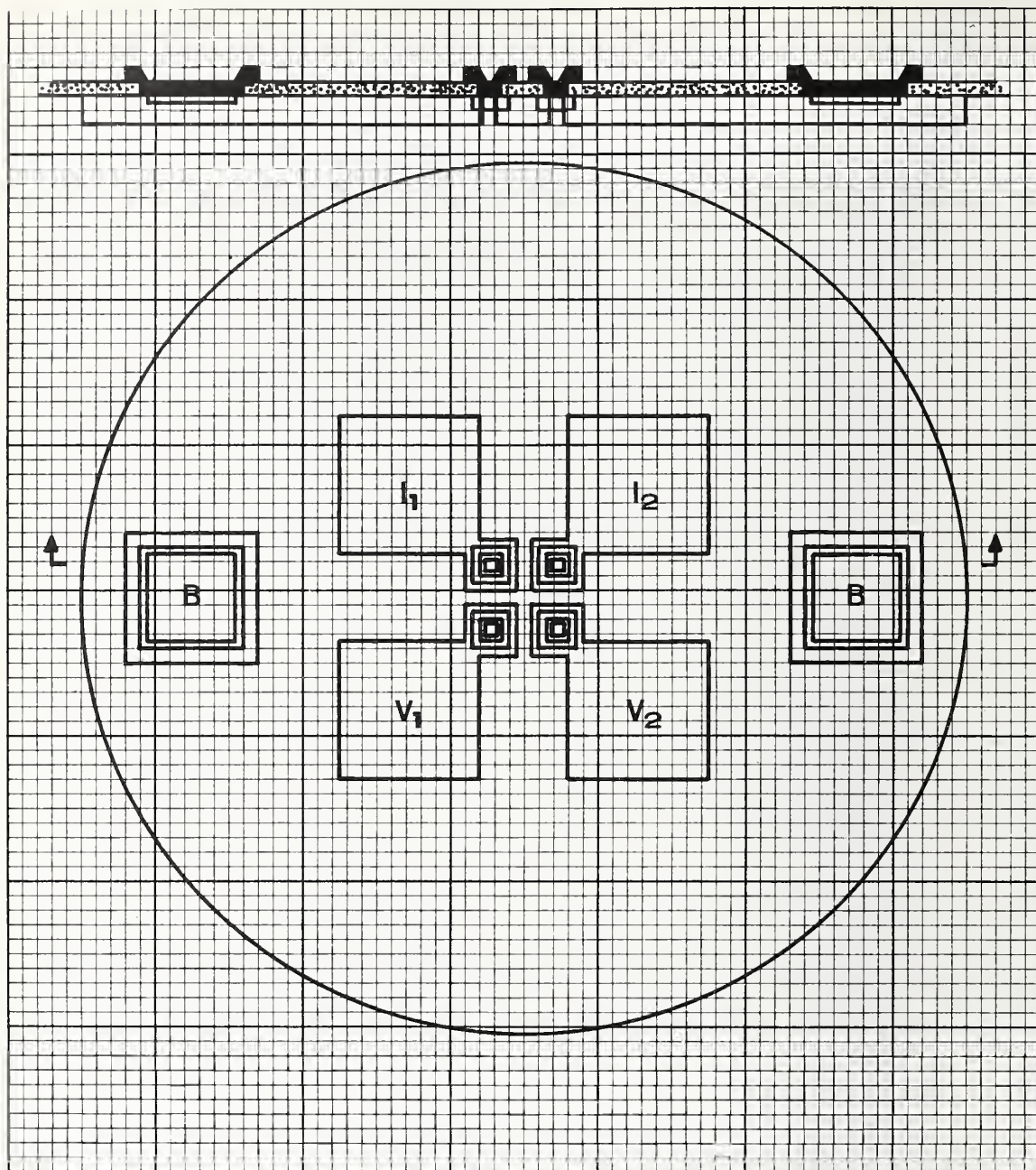
3.14 Metal-to-Base  
Contact Resistor  
Structure 4.29



3.15 Metal-to-Emitter  
Contact Resistor  
Structure 4.27



3.16 Collector Four-Probe Resistors  
 Structure 4.9, pipes 0.50 mil (12.7  $\mu\text{m}$ ) on a side



Other similar structures, which differ primarily in pipe size, are:

Structure 4.1, pipes 0.20 mil (5.1  $\mu\text{m}$ ) on a side

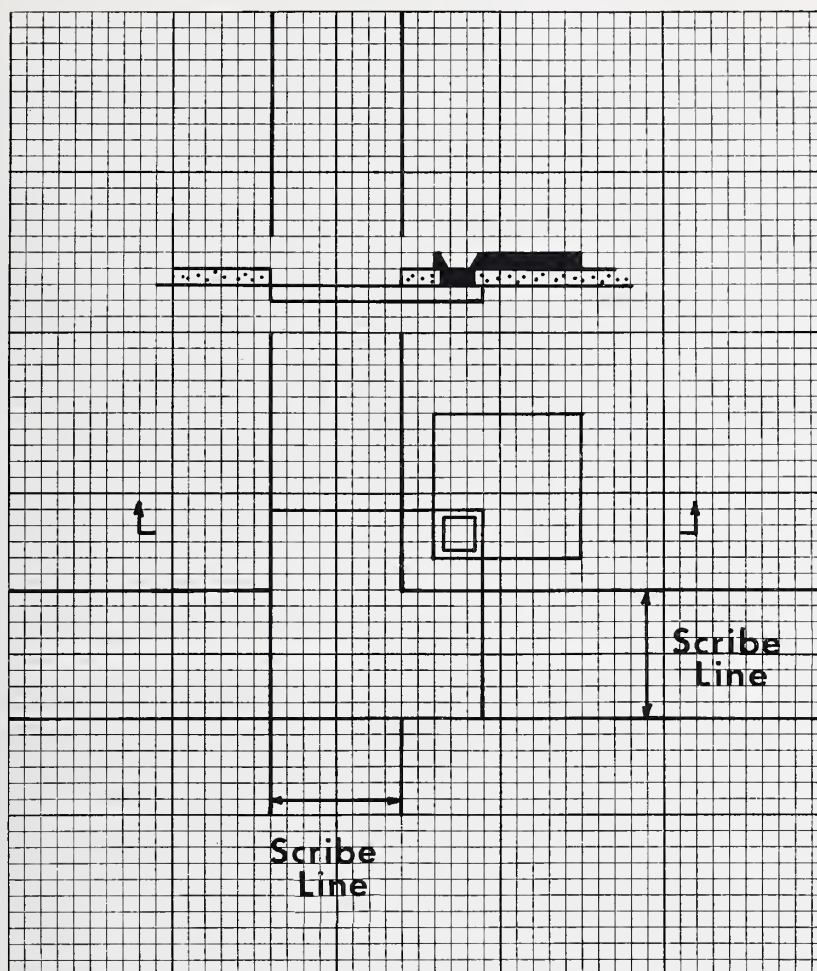
Structure 4.5, pipes 0.30 mil (7.5  $\mu\text{m}$ ) on a side

Structure 4.7, pipes 0.40 mil (10.2  $\mu\text{m}$ ) on a side

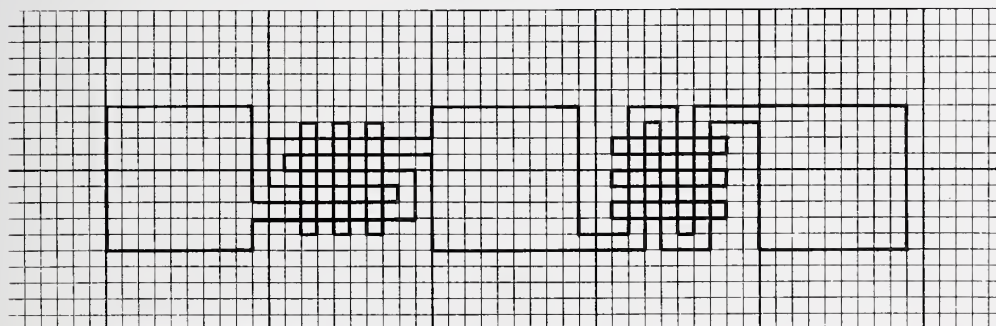
Structure 4.17, pipes 0.25 mil (6.4  $\mu\text{m}$ ) on a side



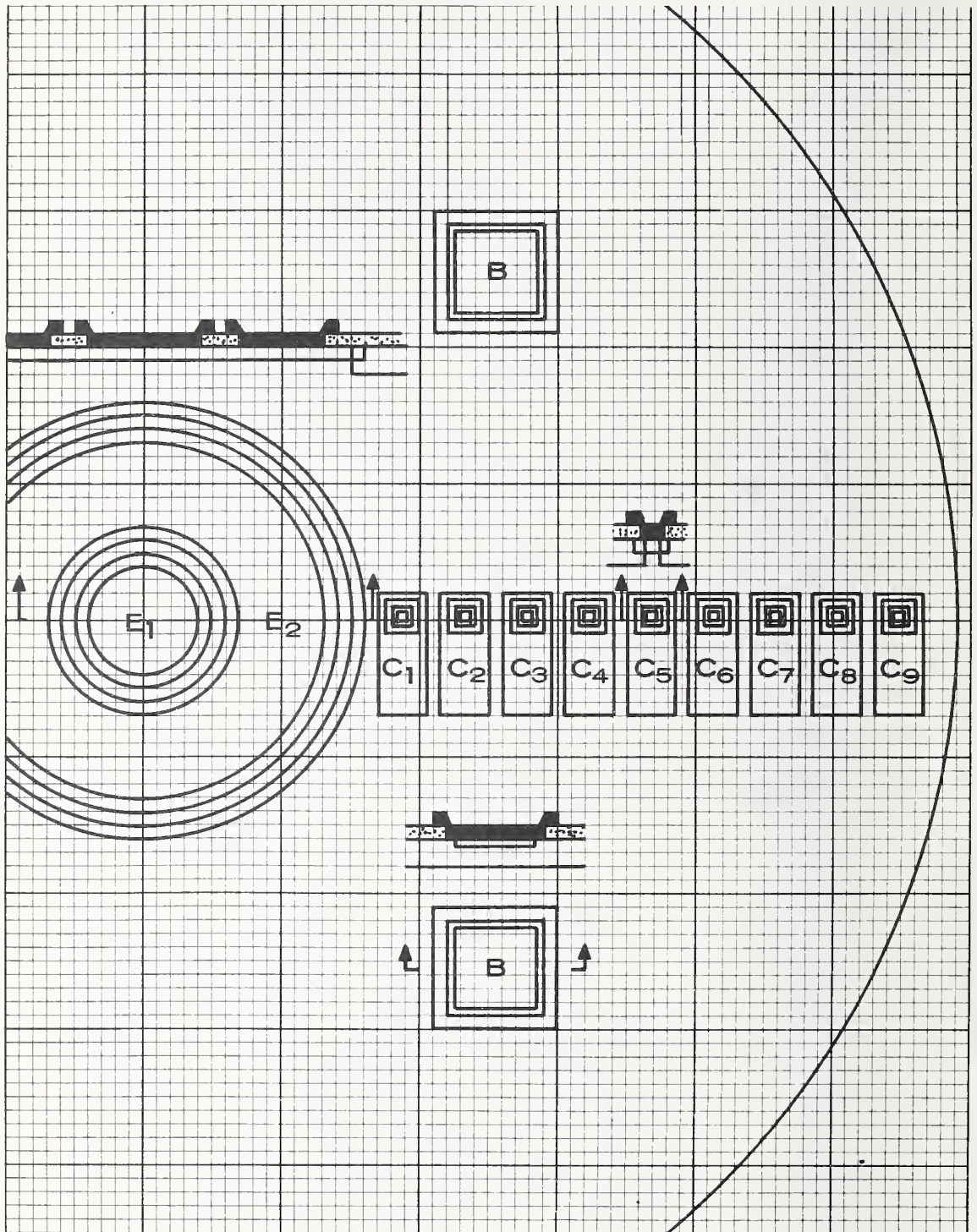
3.17 Collector Hall Effect Device (van der Pauw)  
Structure 4.31



3.18 Metal Step-Coverage Resistor  
Structure 4.38

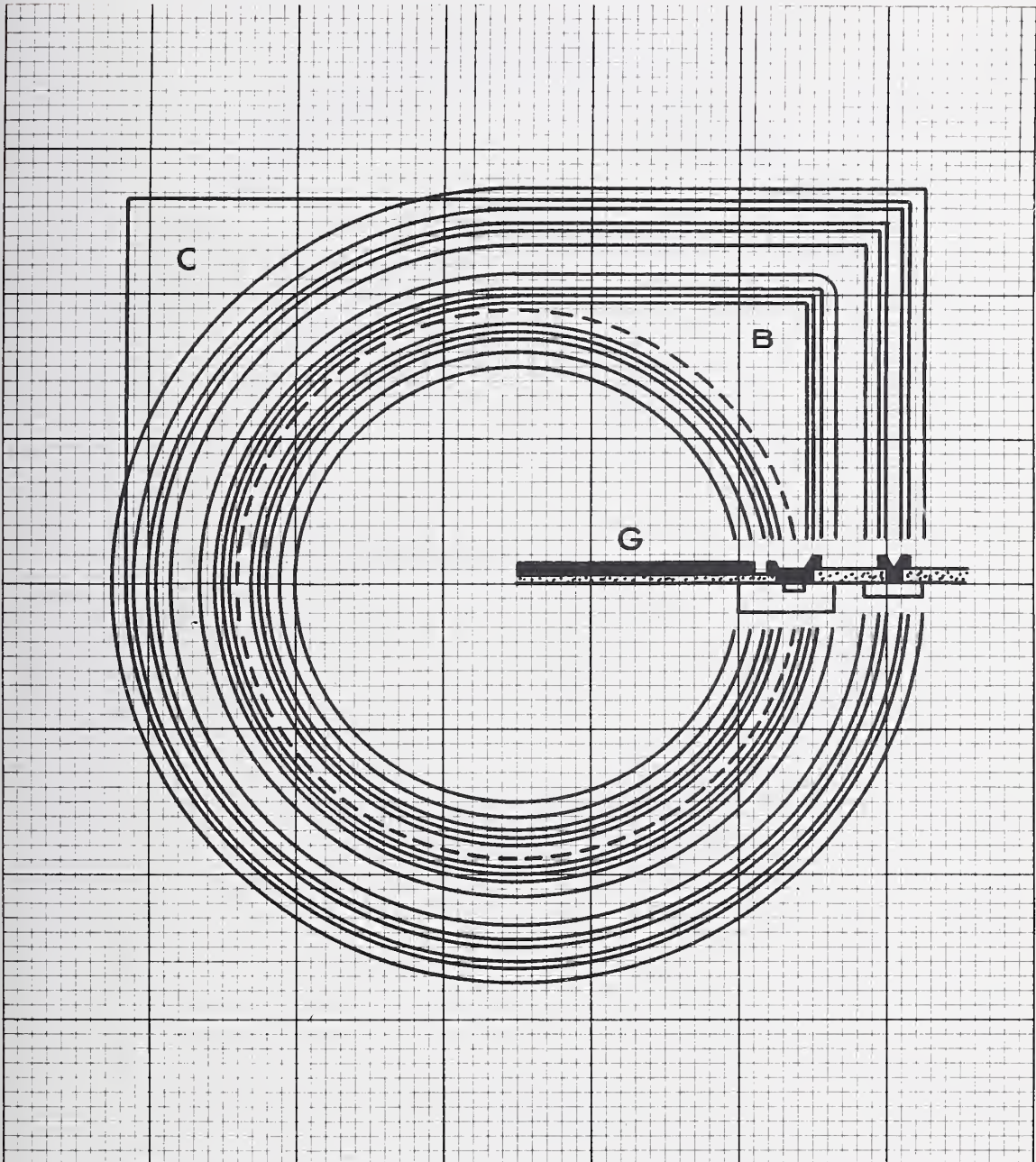


3.19 Collector Spreading Resistor  
Structure 4.18



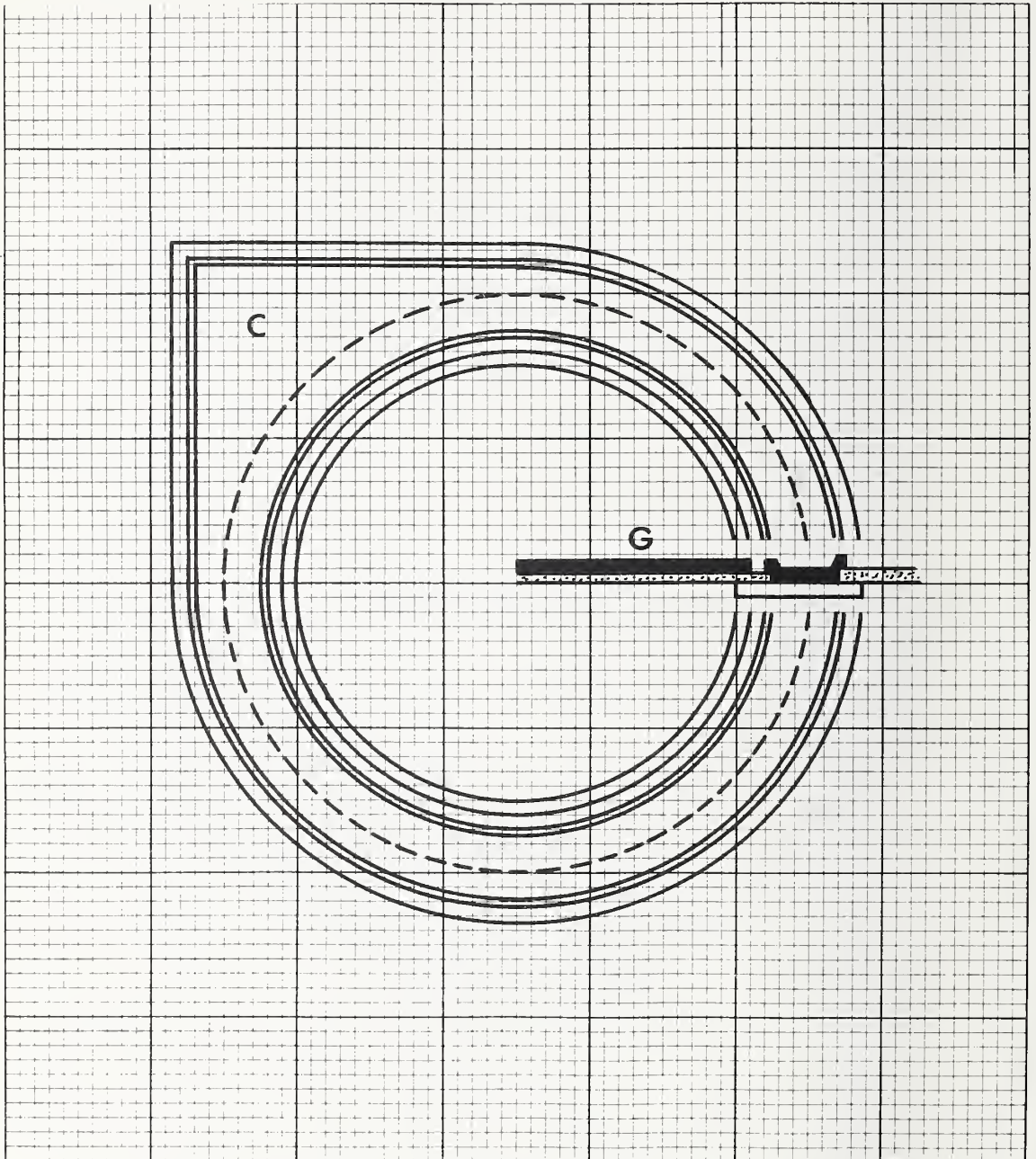
#### 4. MOS CAPACITORS

##### 4.1 MOS Capacitor over Collector (Base DGR, Channel Stop) Structure 4.2

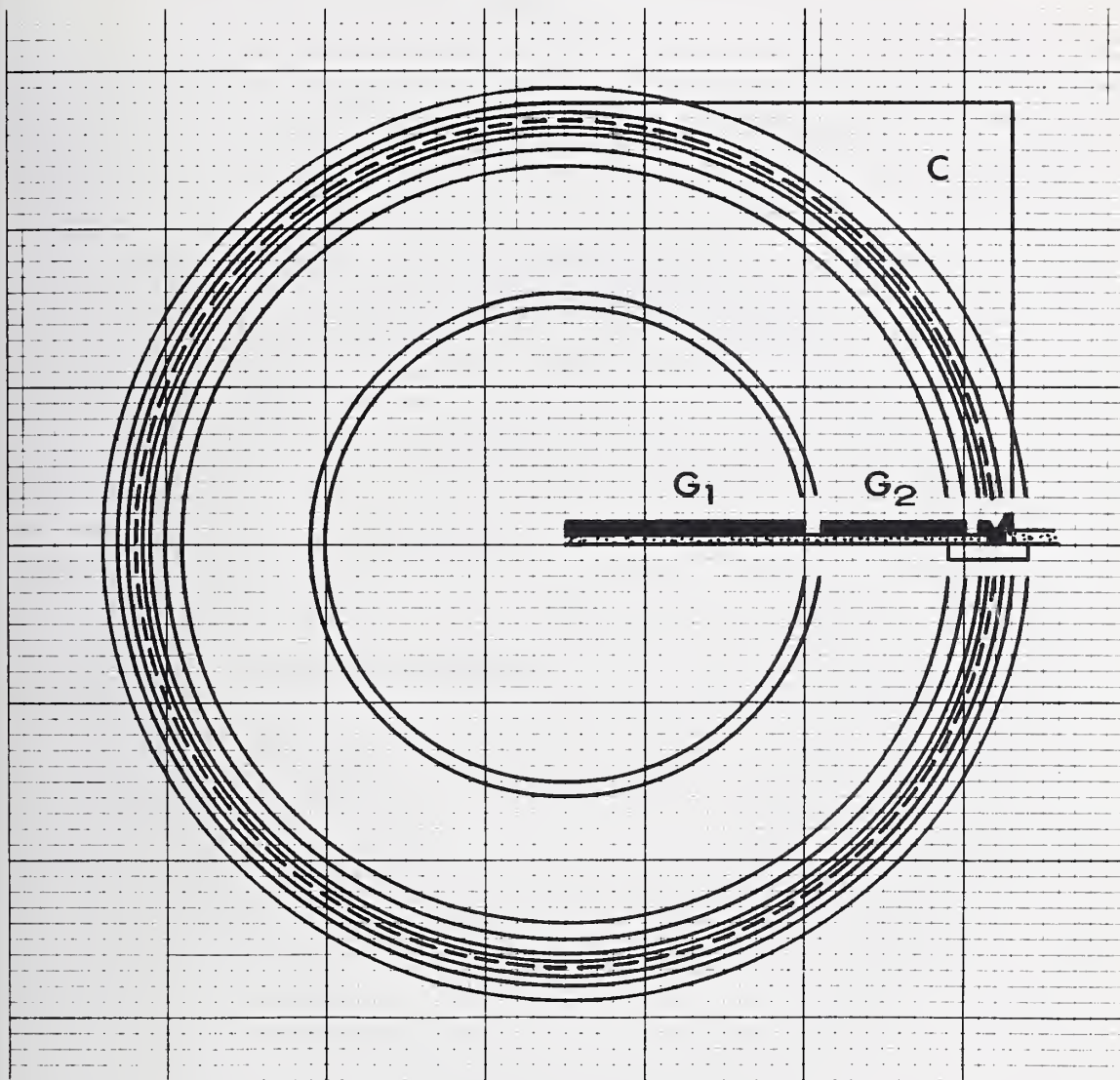




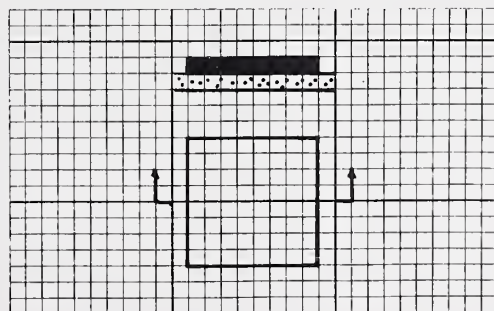
4.2 MOS Capacitor over Collector (Emitter DGR)  
Structure 4.3



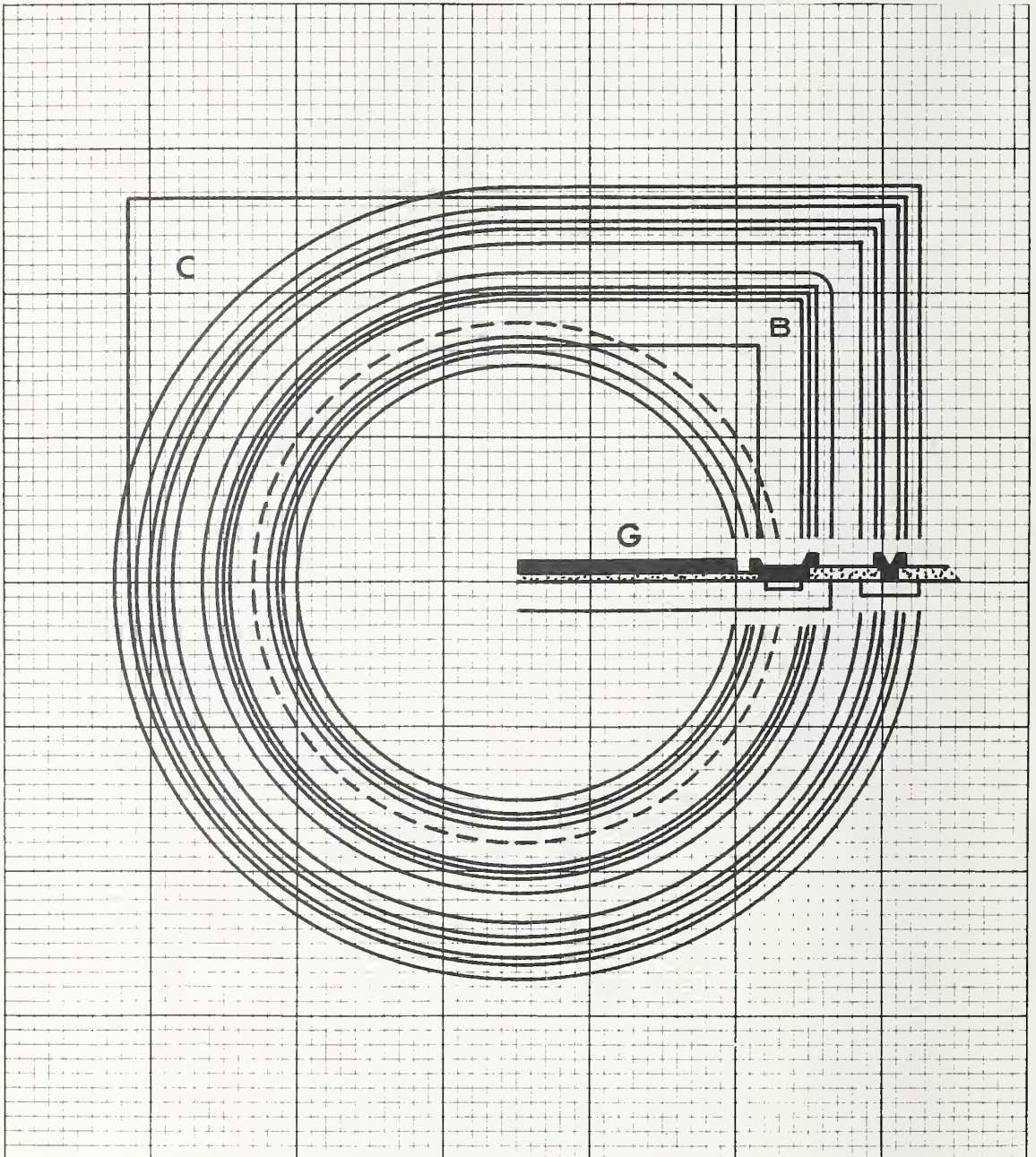
4.3 MOS Capacitor over Collector (Field Plate, Channel Stop)  
Structure 4.8



4.4 MOS Capacitor over Collector  
Structure 4.30



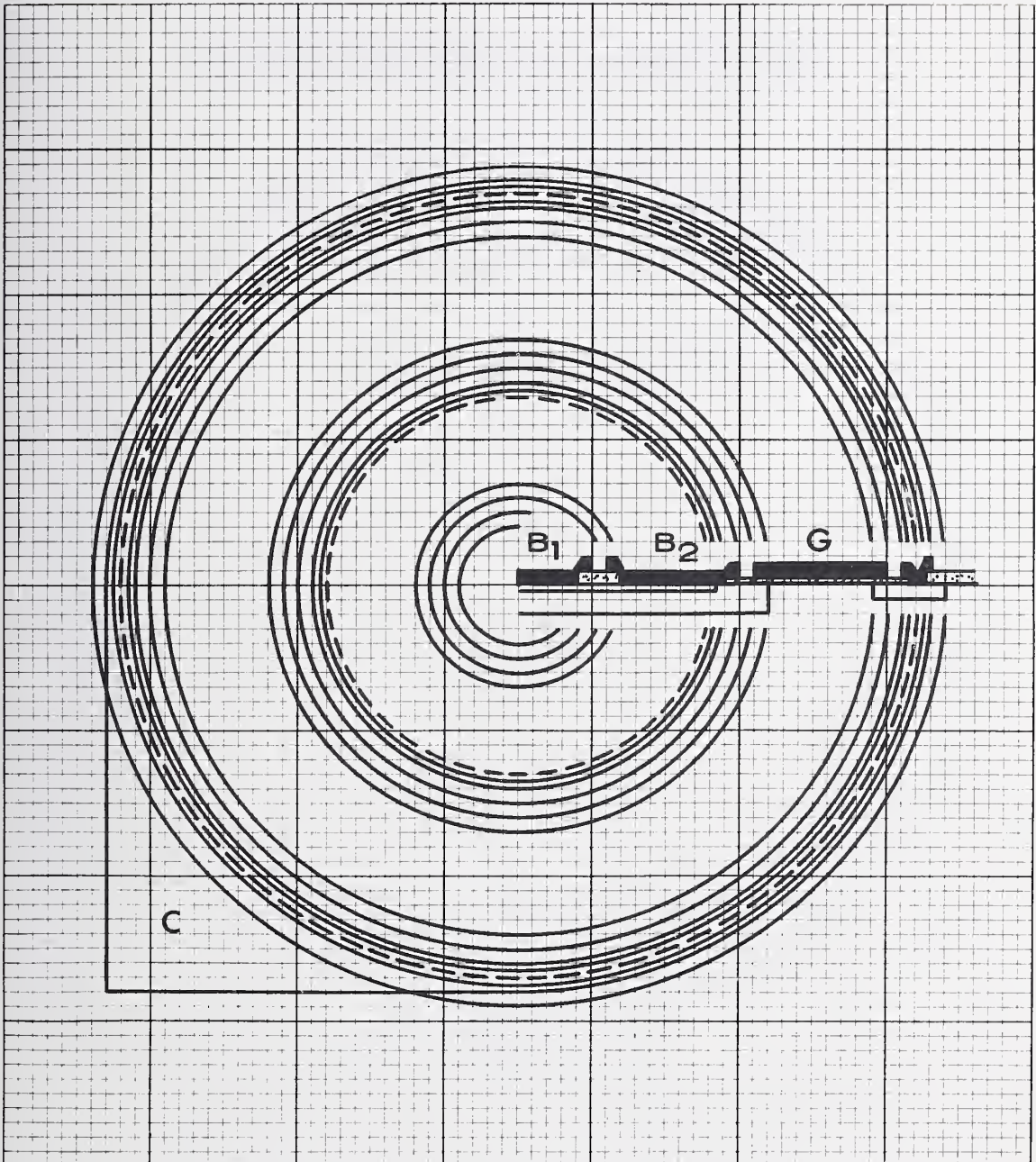
4.5 MOS Capacitor over Base  
Structure 4.12



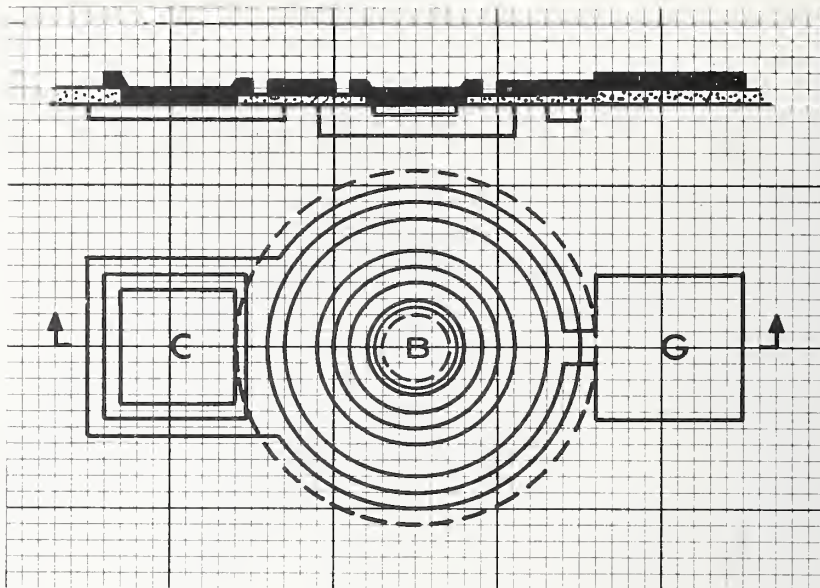


## 5. DIODES

### 5.1 Base-Collector Diode (Field Plate, Channel Stop) Structure 4.10

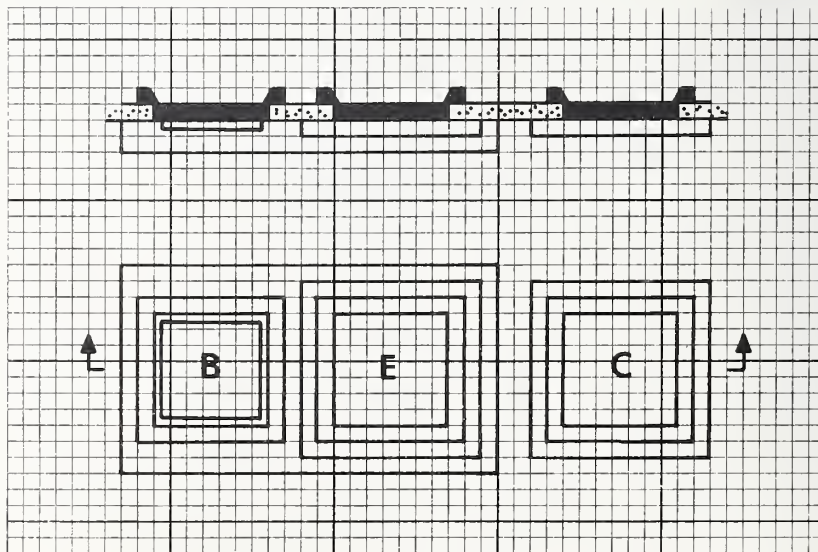


5.2 Base-Collector Diode (Field Plate, Channel Stop)  
Structure 4.14



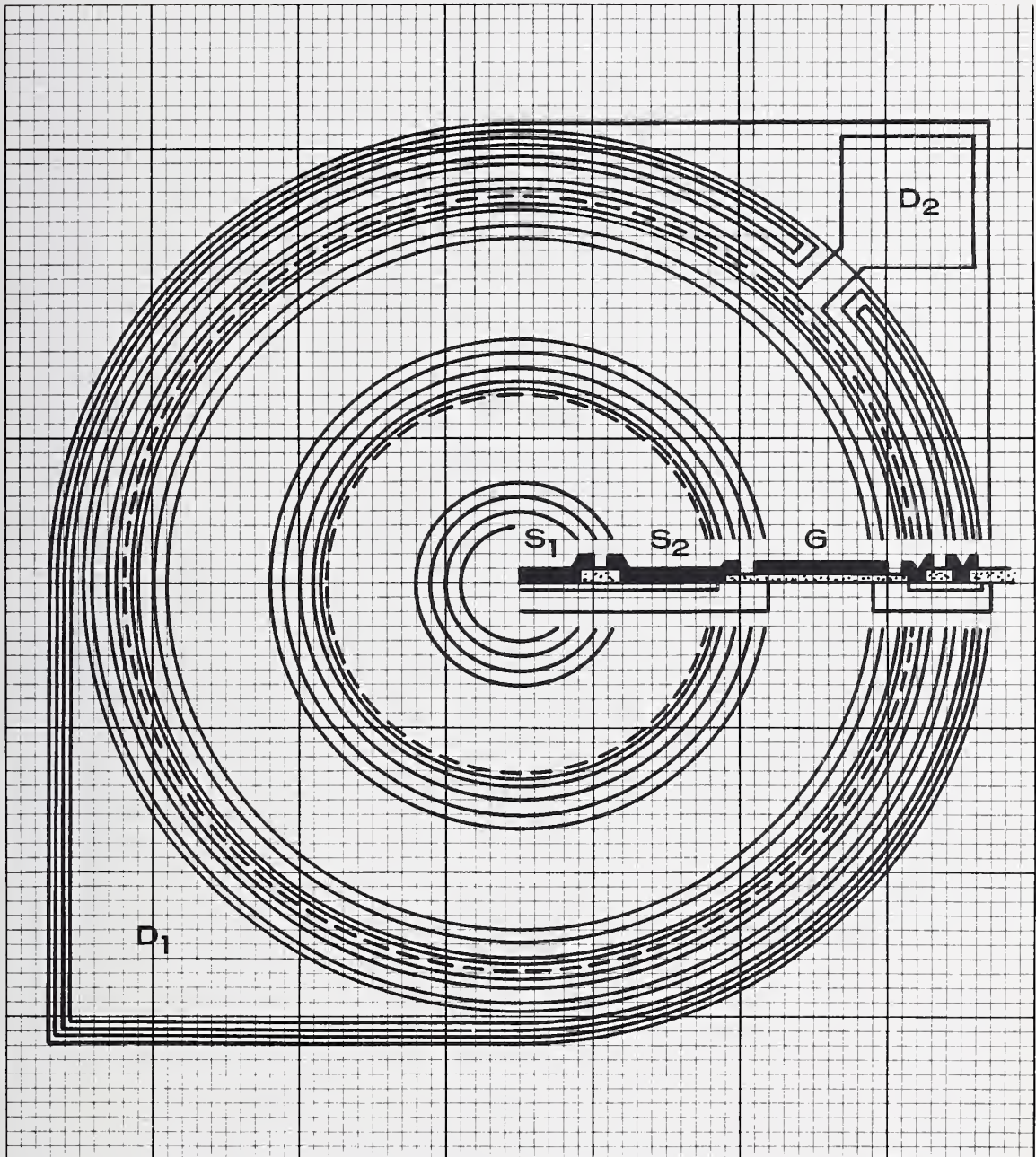
6. TRANSISTORS

6.1 Bipolar Transistor  
Structure 4.13

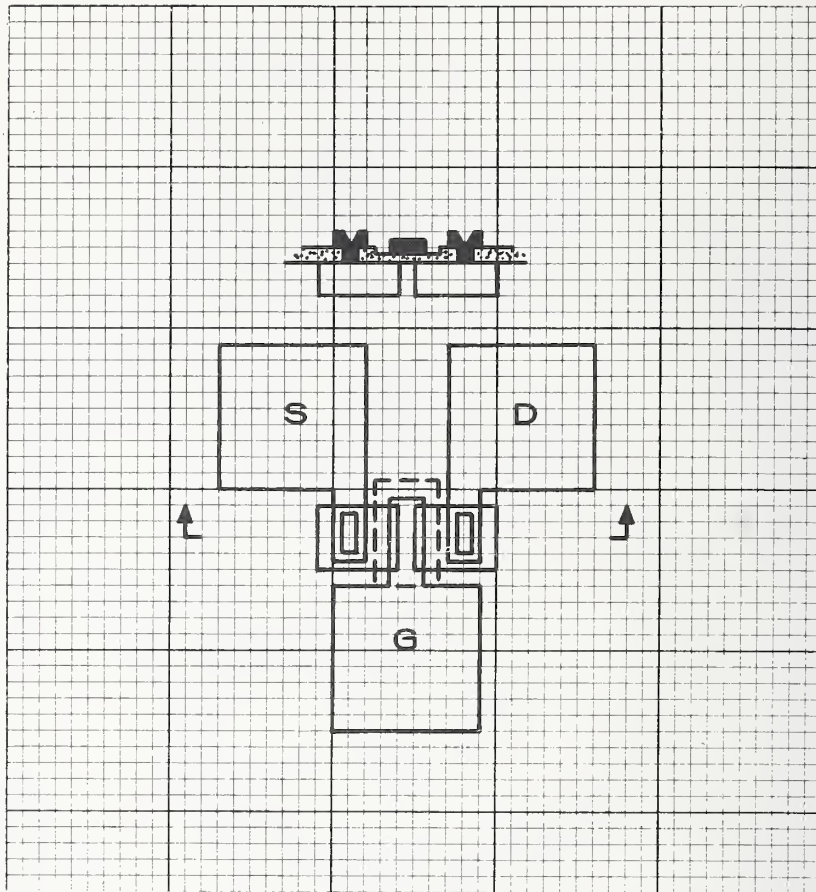




6.2 MOS Transistor (Circular)  
Structure 4.15

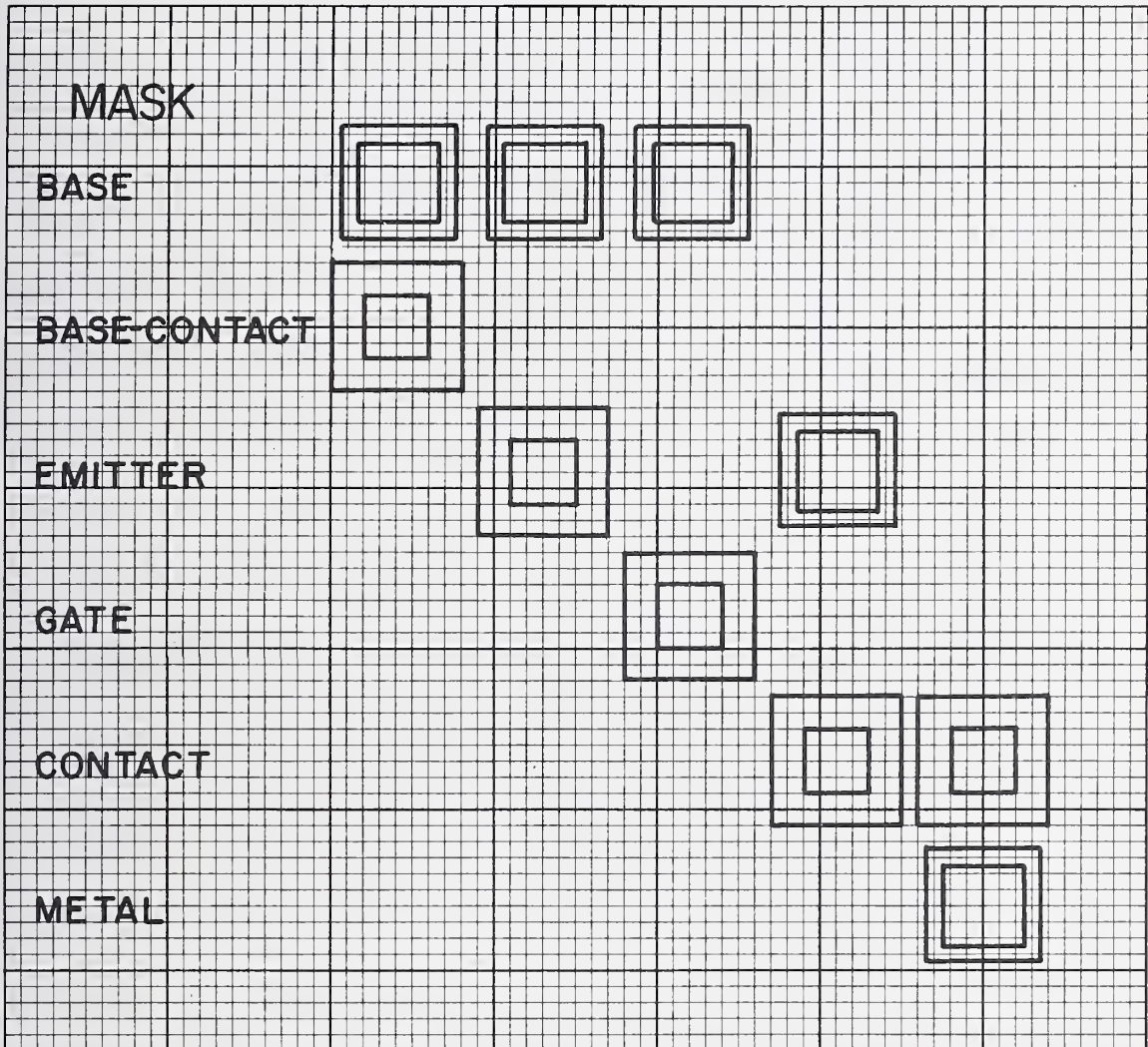


6.3 MOS Transistor  
Structure 4.16



## 7. MISCELLANEOUS

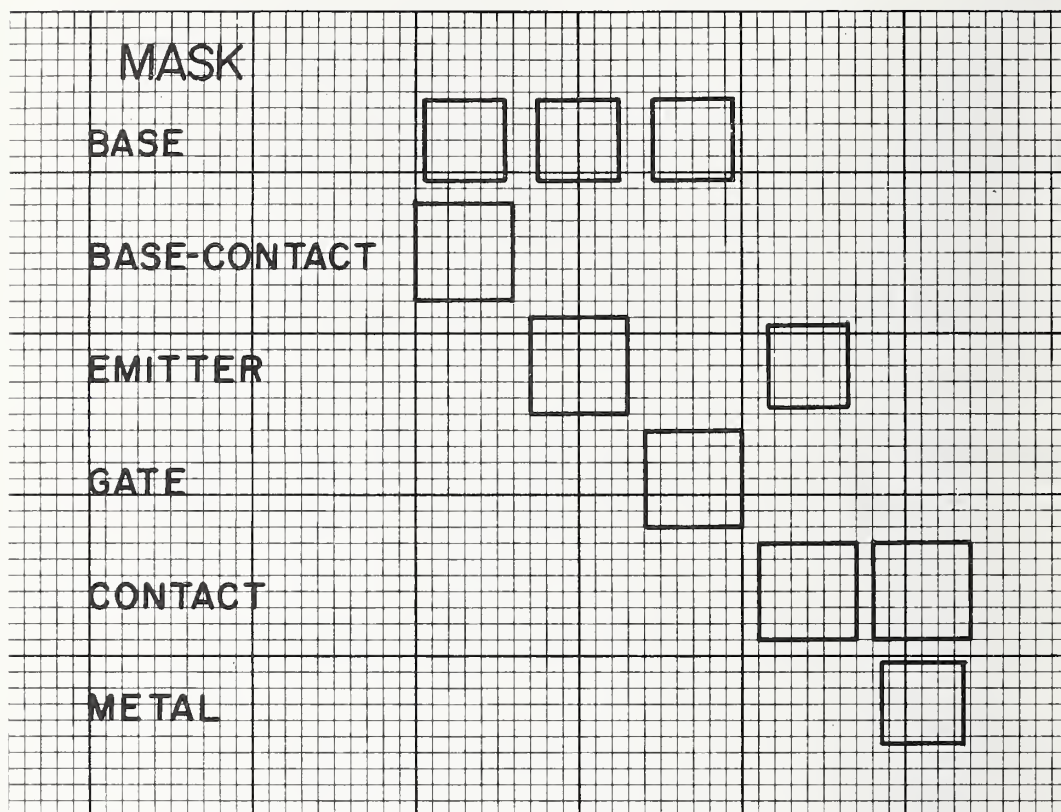
### 7.1 Alignment Markers for Negative Photoresist<sup>\*</sup> Structure 4.4 N



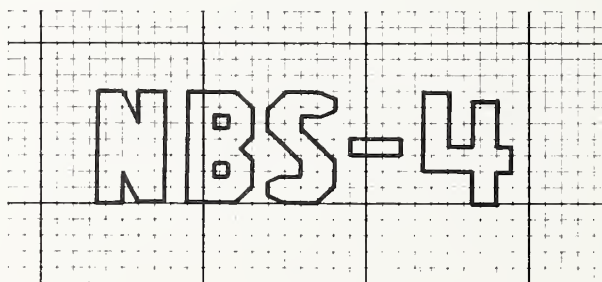
<sup>\*</sup> This structure will also work with positive photoresist.



7.2 Alignment Markers for Positive Photoresist  
Structure 4.4 P

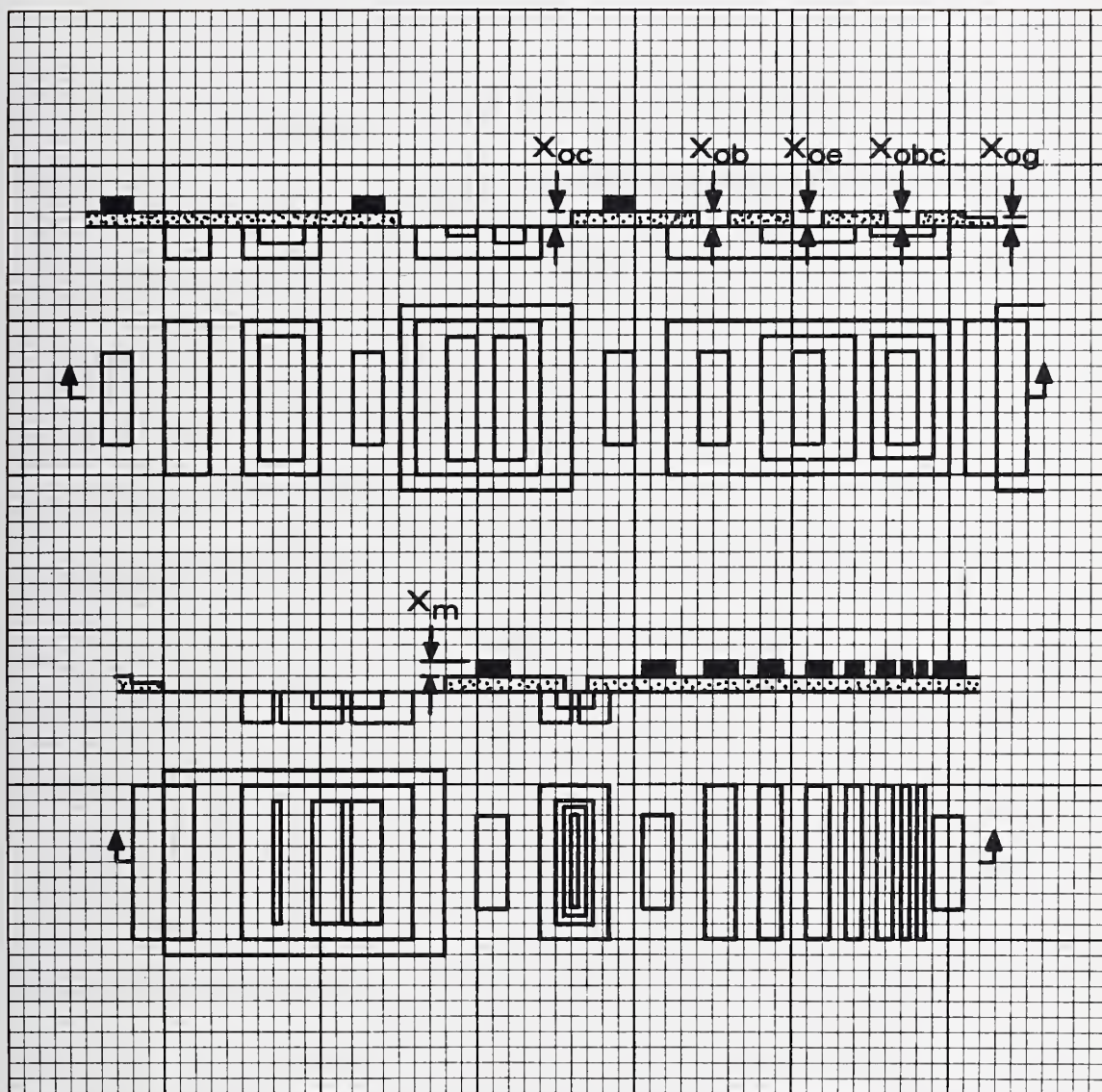


7.3 NBS Logo  
Structure 4.6

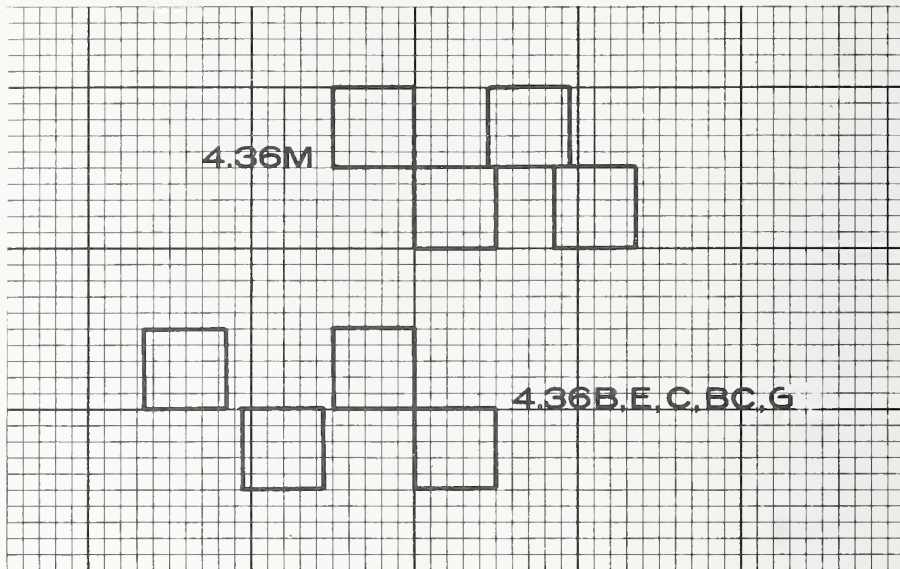




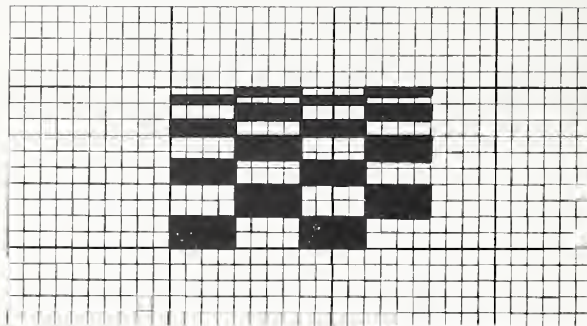
7.4 Surface Profilometer Structure  
Structure 4.34



7.5 Etch Control Structures  
Structures 4.36 B, E, C, M, BC, G



7.6 Resolution Structures  
Structures 4.37 B, E, C, M, BC, G



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14. Chwang, R., Smith, B. J., and Crowell, C. R., Contact Size Effects on the van der Pauw Method for Resistivity and Hall Coefficient Measurements, *Solid-State Electronics* 17, 1217-1227 (1974).



## APPENDIX

In the following figures, the center-to-center distance between the scribe lines is 100 mil (2.54 mm). For all masks except the METAL mask the areas delineated for subsequent diffusion, oxidation, or oxide removal appear white in the photomicrographs of the masks. On the METAL mask the metallization pattern is black on a white background.

Table 2 - Test Structures Shown in Figures 3-9.

Number	Test Structure
4.1	Collector resistor (pipes 0.20 mil on a side)
4.2	MOS capacitor over collector (base DGR)
4.3	MOS capacitor over collector (emitter DGR)
4.4	Alignment markers
4.5	Collector resistor (pipes 0.30 mil on a side)
4.6	Logo
4.7	Collector resistor (pipes 0.40 mil on a side)
4.8	MOS capacitor over collector (FP, CS)
4.9	Collector resistor (pipes 0.50 mil on a side)
4.10	Base-collector diode (FP, CS)
4.11	Base sheet resistor (VDP, FP, CS)

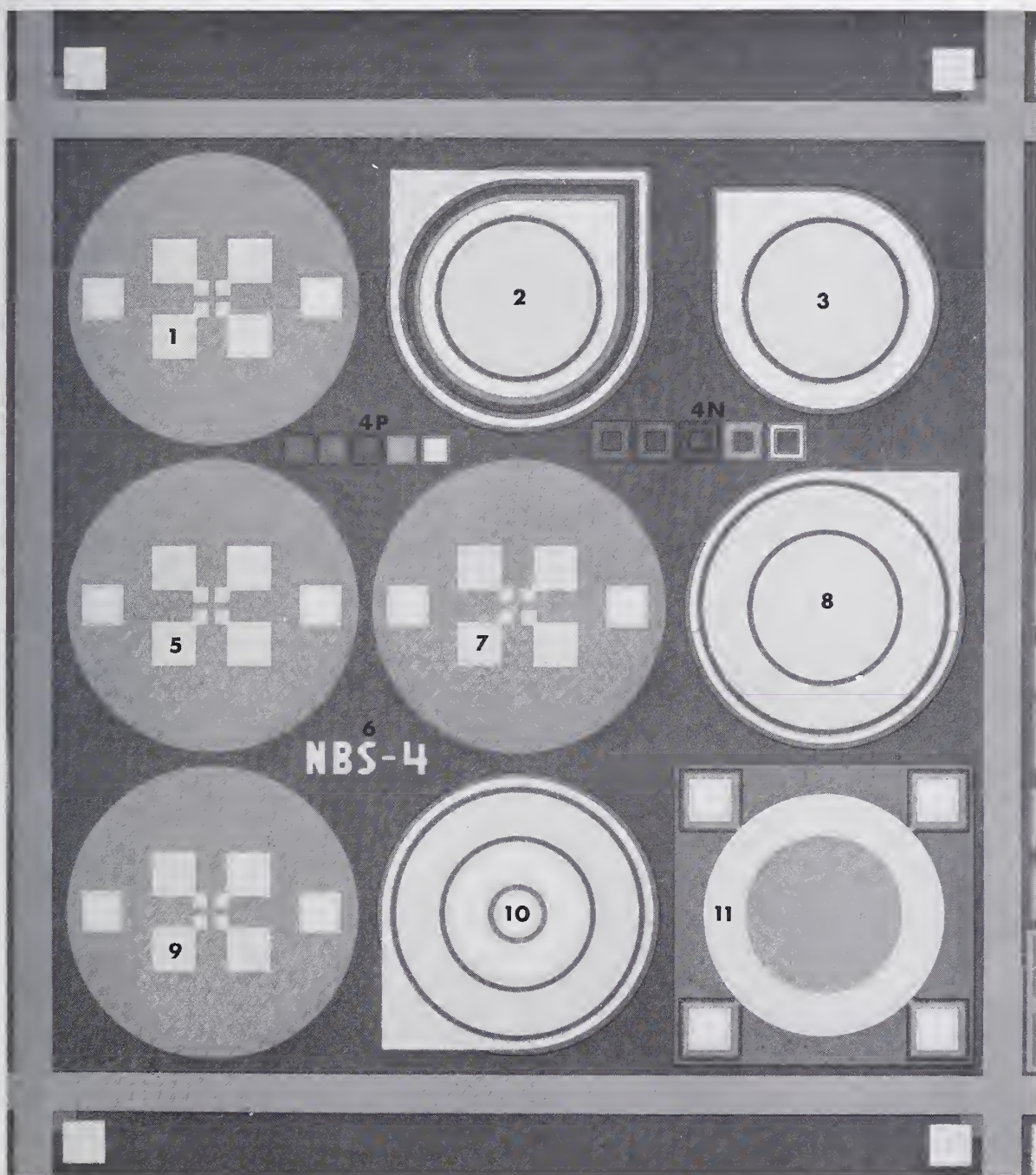


Figure 3. Quadrant 1 of test pattern NBS-4. Test structures are identified in table 2.





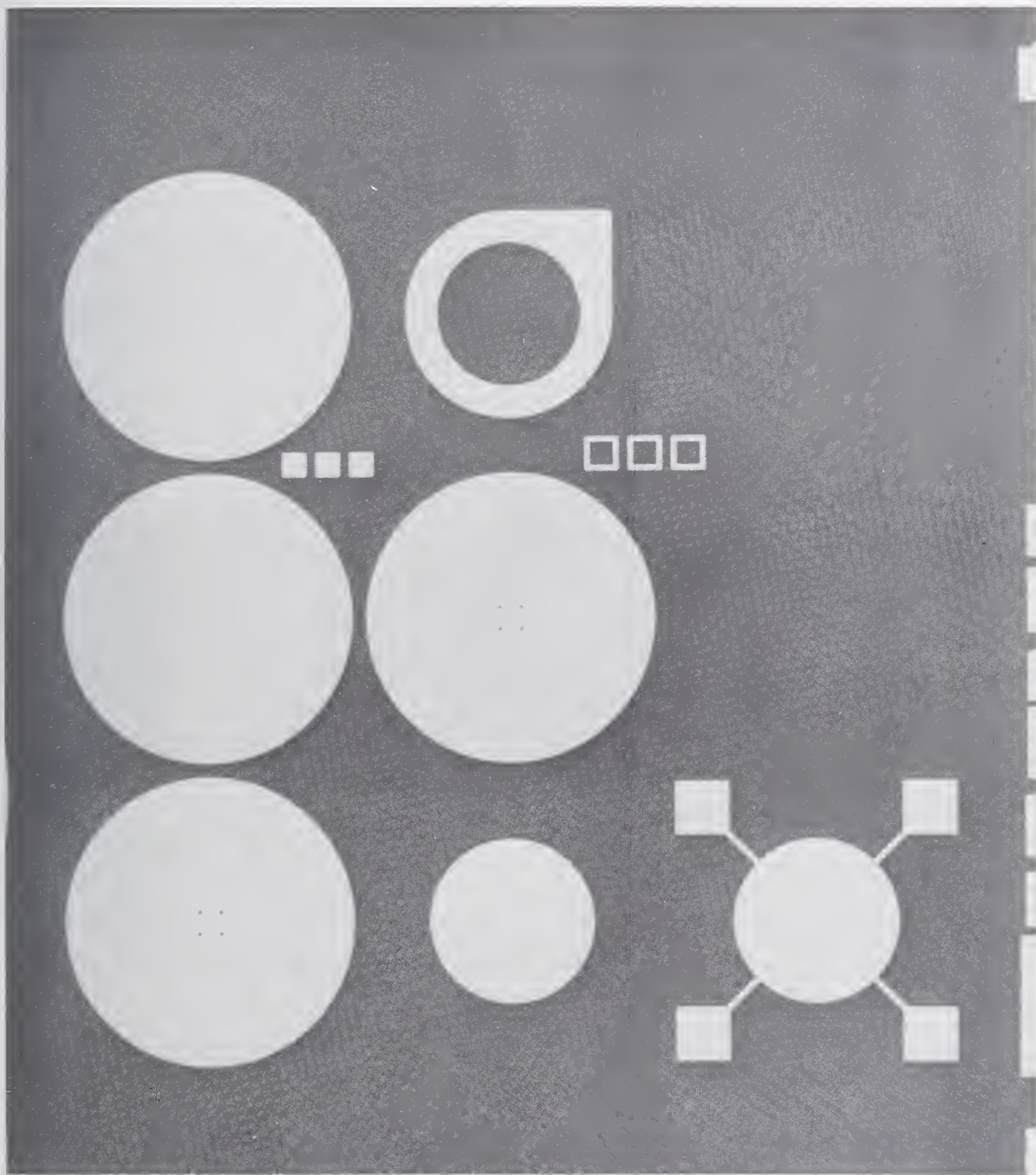


Figure 4. BASE mask for quadrant 1 of test pattern NBS-4. Test structures located in this quadrant are listed in table 2.



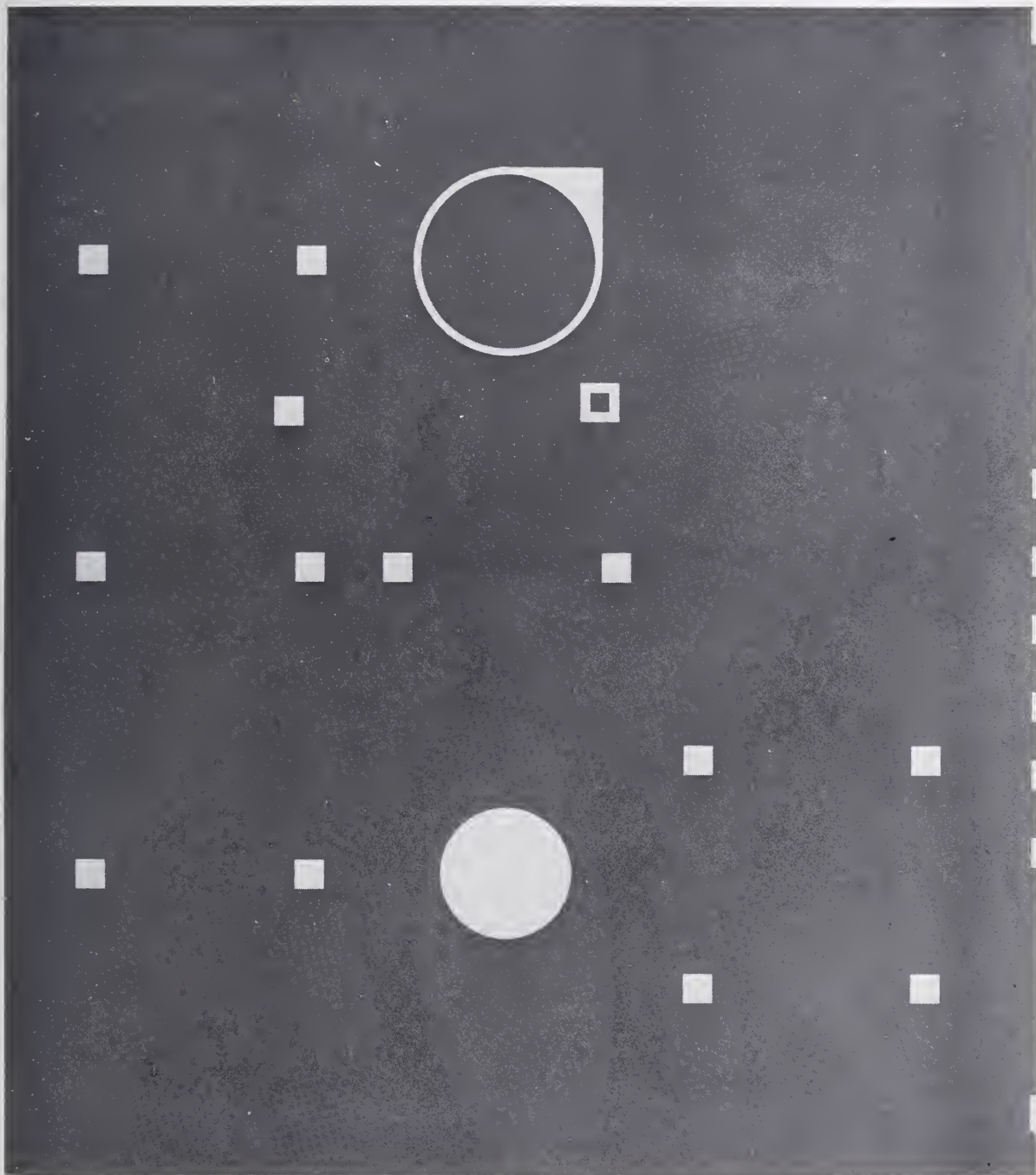


Figure 5. BASE-CONTACT mask for quadrant 1 of test pattern NBS-4. Test structures located in this quadrant are listed in table 2.





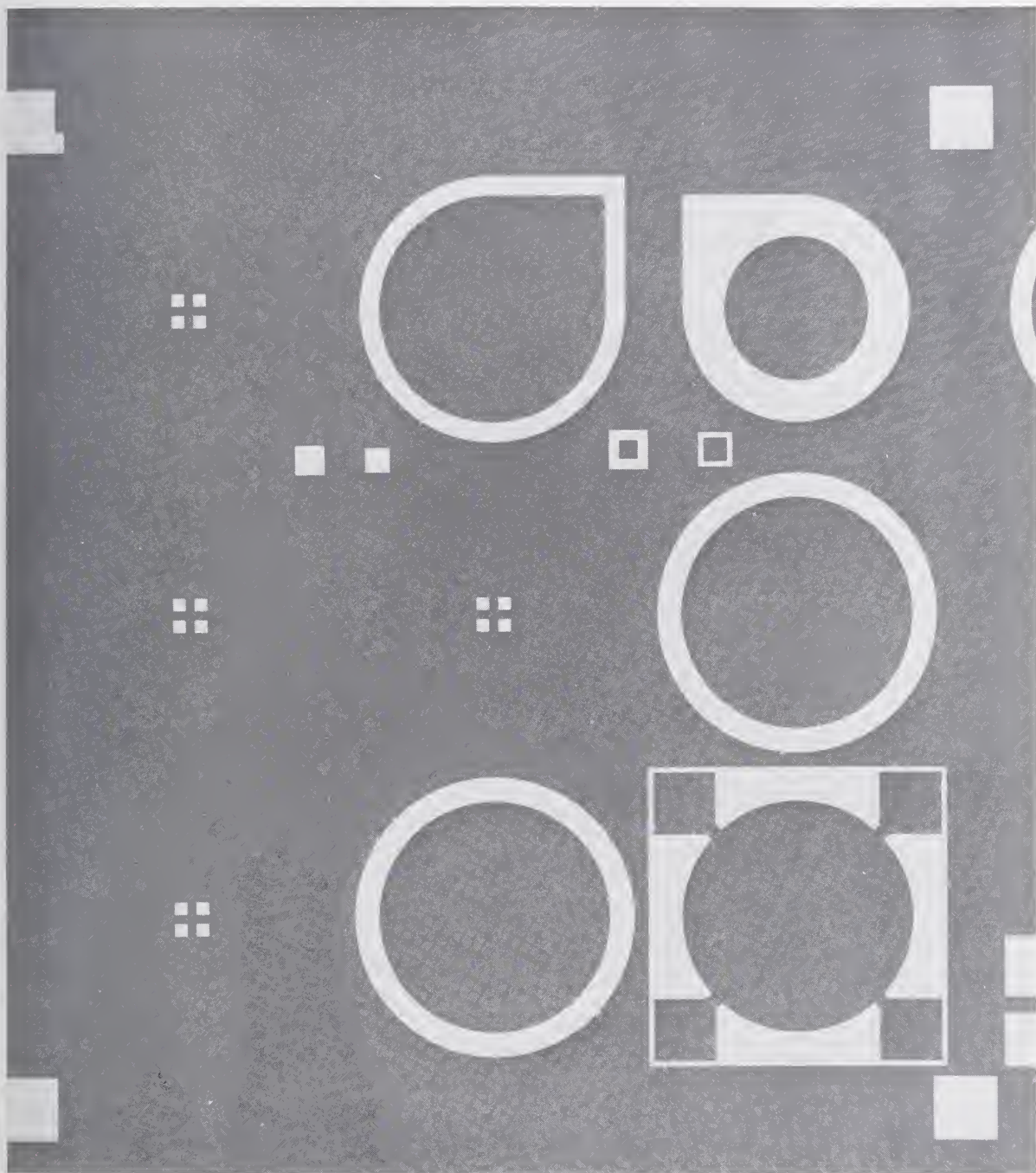


Figure 6. EMITTER mask for quadrant 1 of test pattern NBS-4. Test structures located in this quadrant are listed in table 2.





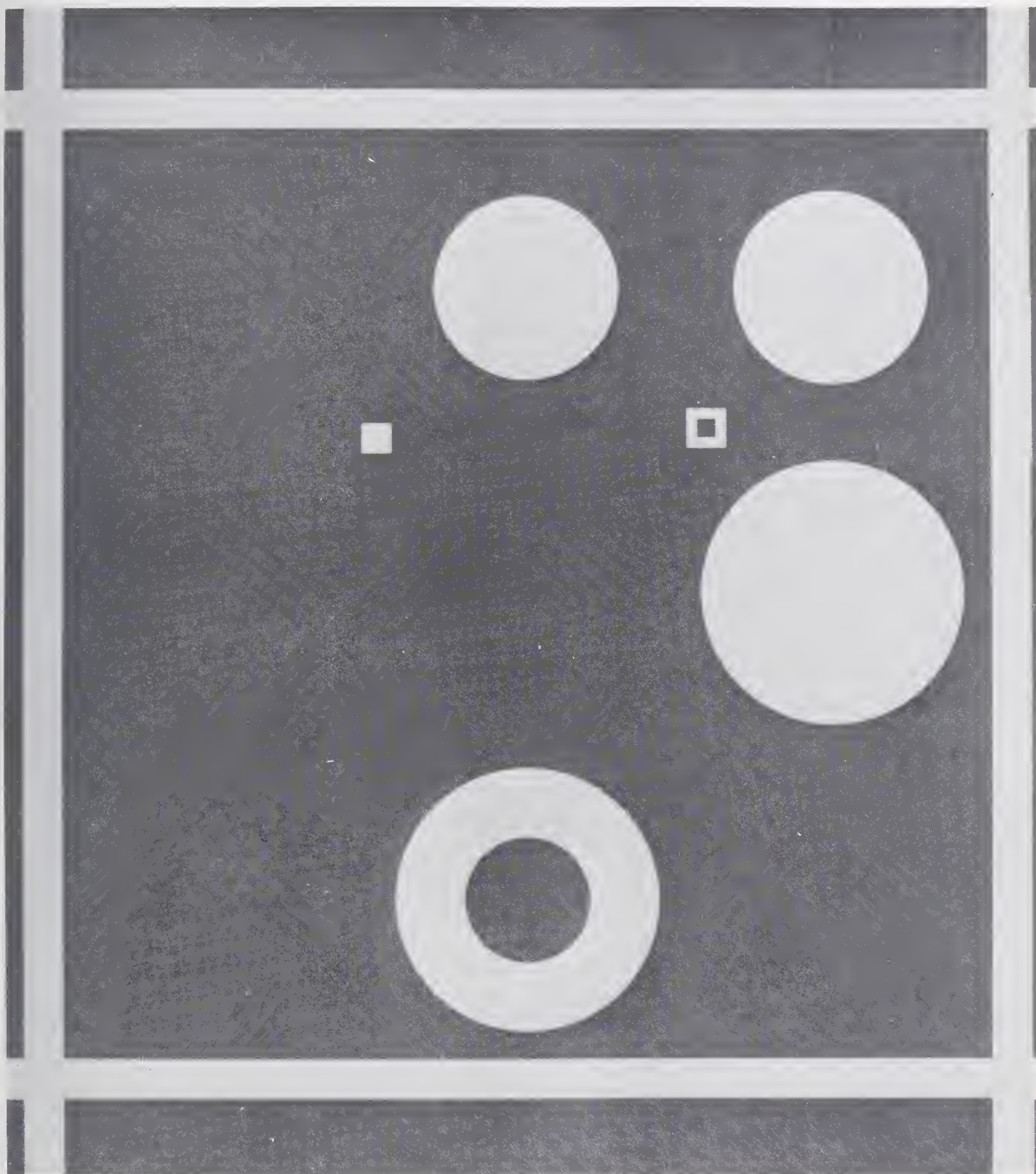


Figure 7. GATE mask for quadrant 1 of test pattern NBS-4. Test structures located in this quadrant are listed in table 2.



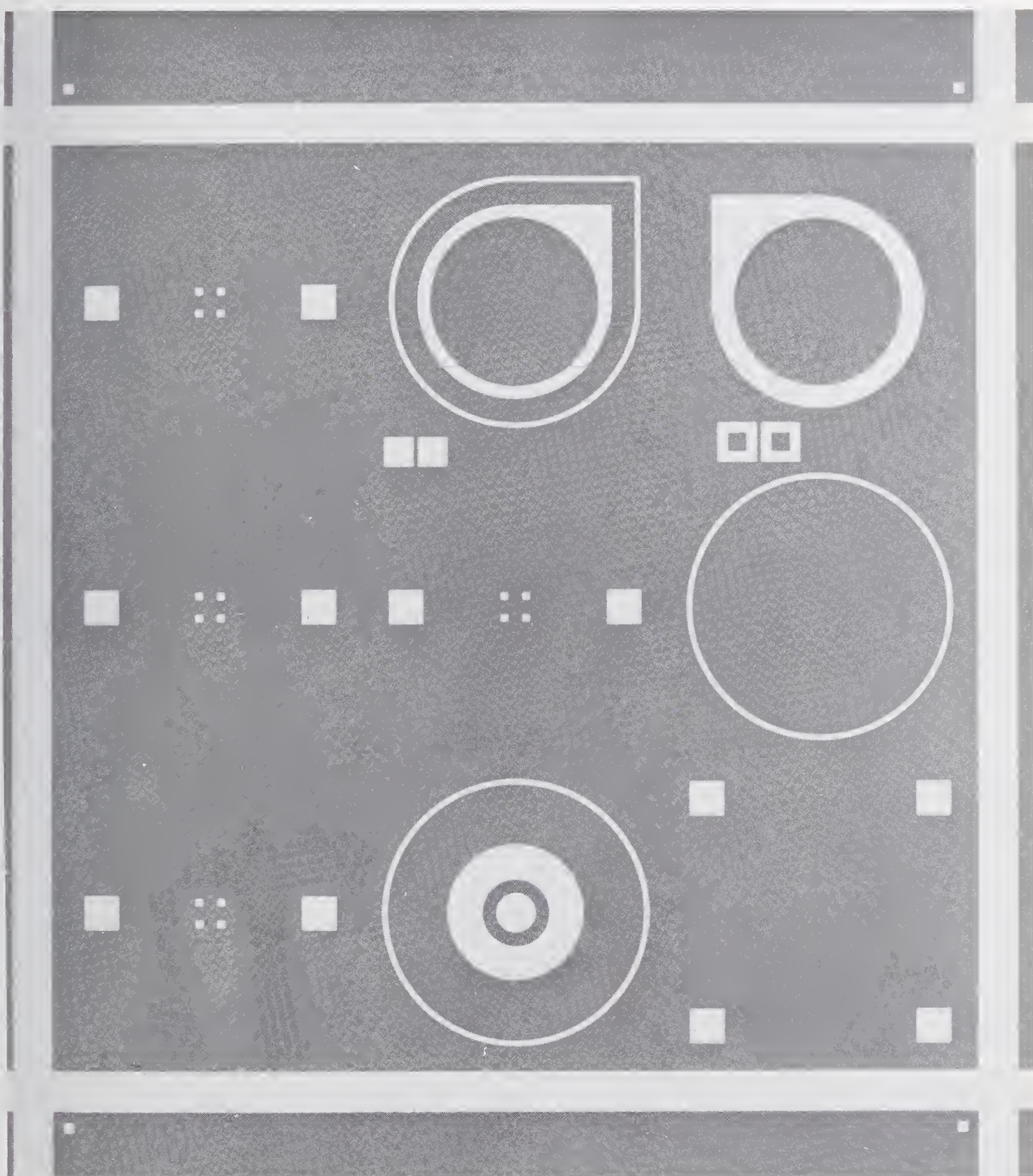


Figure 8. CONTACT mask for quadrant 1 of test pattern NBS-4. Test structures located in this quadrant are listed in table 2.





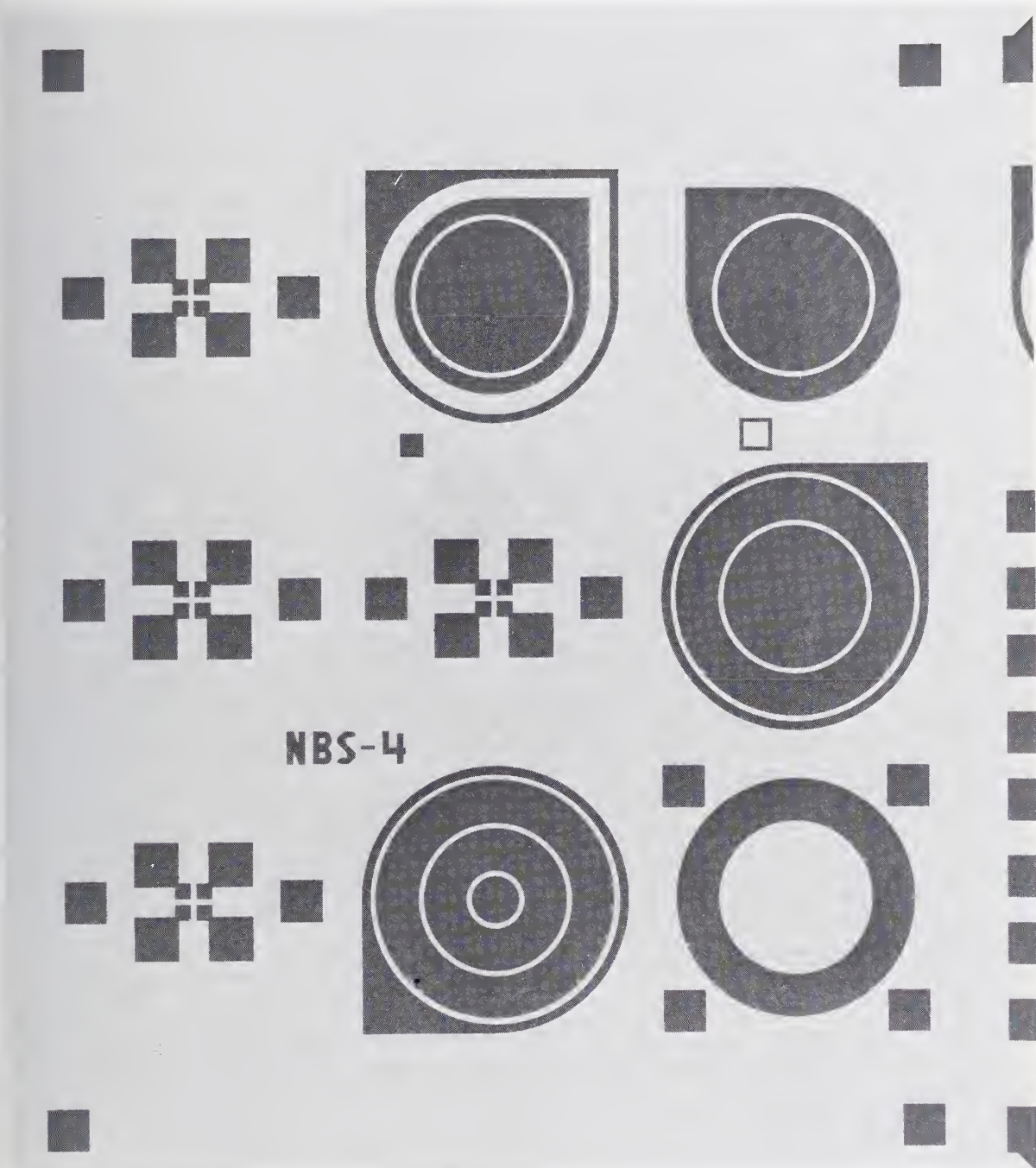


Figure 9. METAL mask for quadrant 1 of test pattern NBS-4. Test structures located in this quadrant are listed in table 2.

Table 3 - Test Structures Shown in Figures 10-16.

Number	Test Structure
4.12	MOS Capacitor over base
4.13	Bipolar transistor
4.14	Base-collector diode (FP, CS)
4.15	MOSFET (circular, W/L = 18.2)
4.16	MOSFET (rectangular, W/L = 4)
4.17	Collector resistor (pipes 0.25 mil on a side)
4.18	Collector spreading resistor
4.19	Metal sheet resistor (Greek cross)
4.20	Base-under-emitter sheet resistor (Greek cross)
4.21	Base-contact sheet resistor (Greek cross)
4.22	Base sheet resistor (narrow Greek cross)
4.23	Base sheet resistor (bridge, W/L = 0.25)
4.24	Base sheet resistor (Greek cross)
4.25	Base sheet resistor (Greek cross, tab contacts)
4.26	Base sheet resistor (offset quadrate cross)
4.27	Metal-to-emitter contact resistor
4.28	Emitter sheet resistor (offset quadrate cross)
4.29	Metal-to-base contact resistor
4.30	MOS capacitor over collector (square)



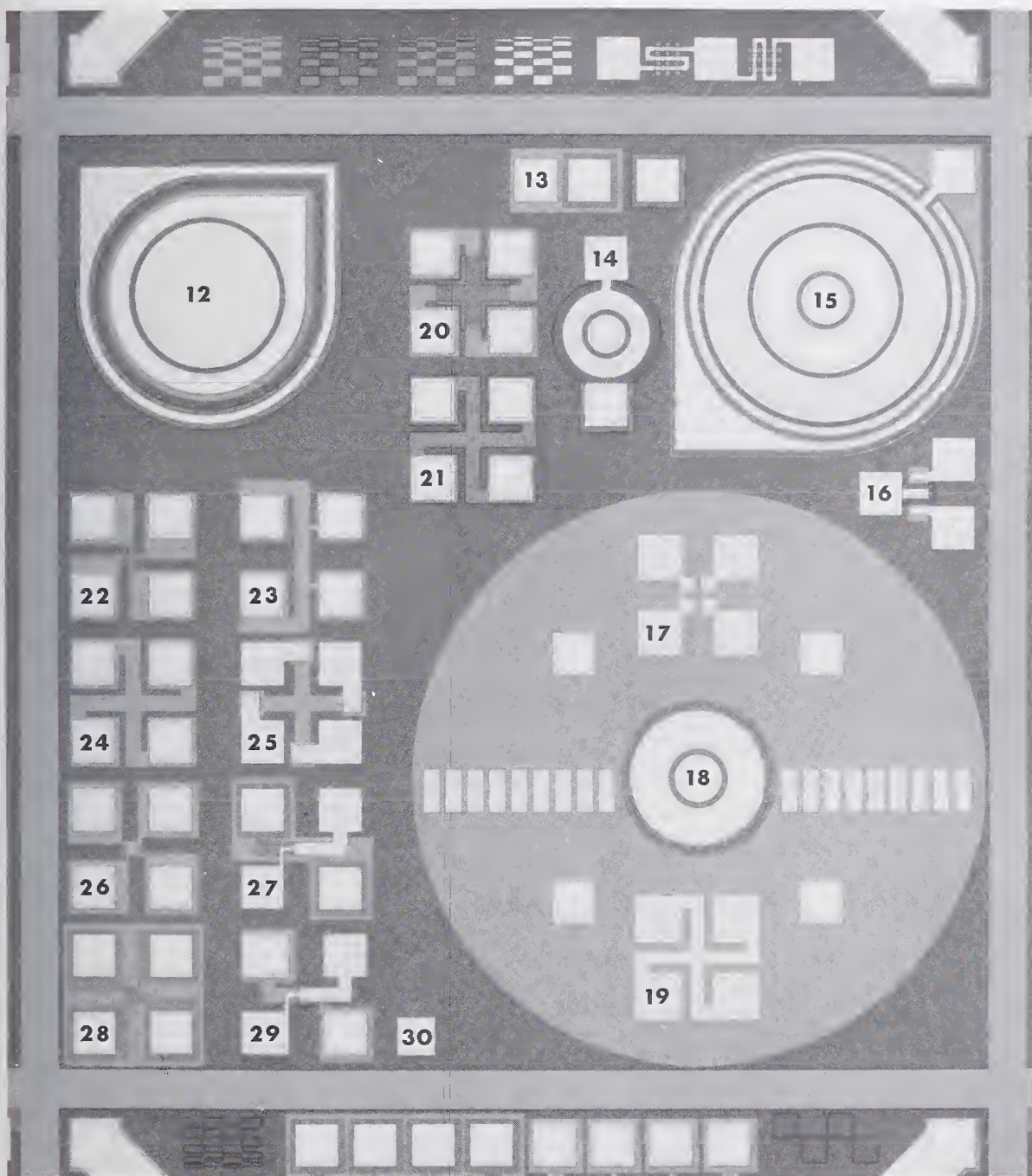


Figure 10. Quadrant 2 of test pattern NBS-4. Test structures are identified in table 3.



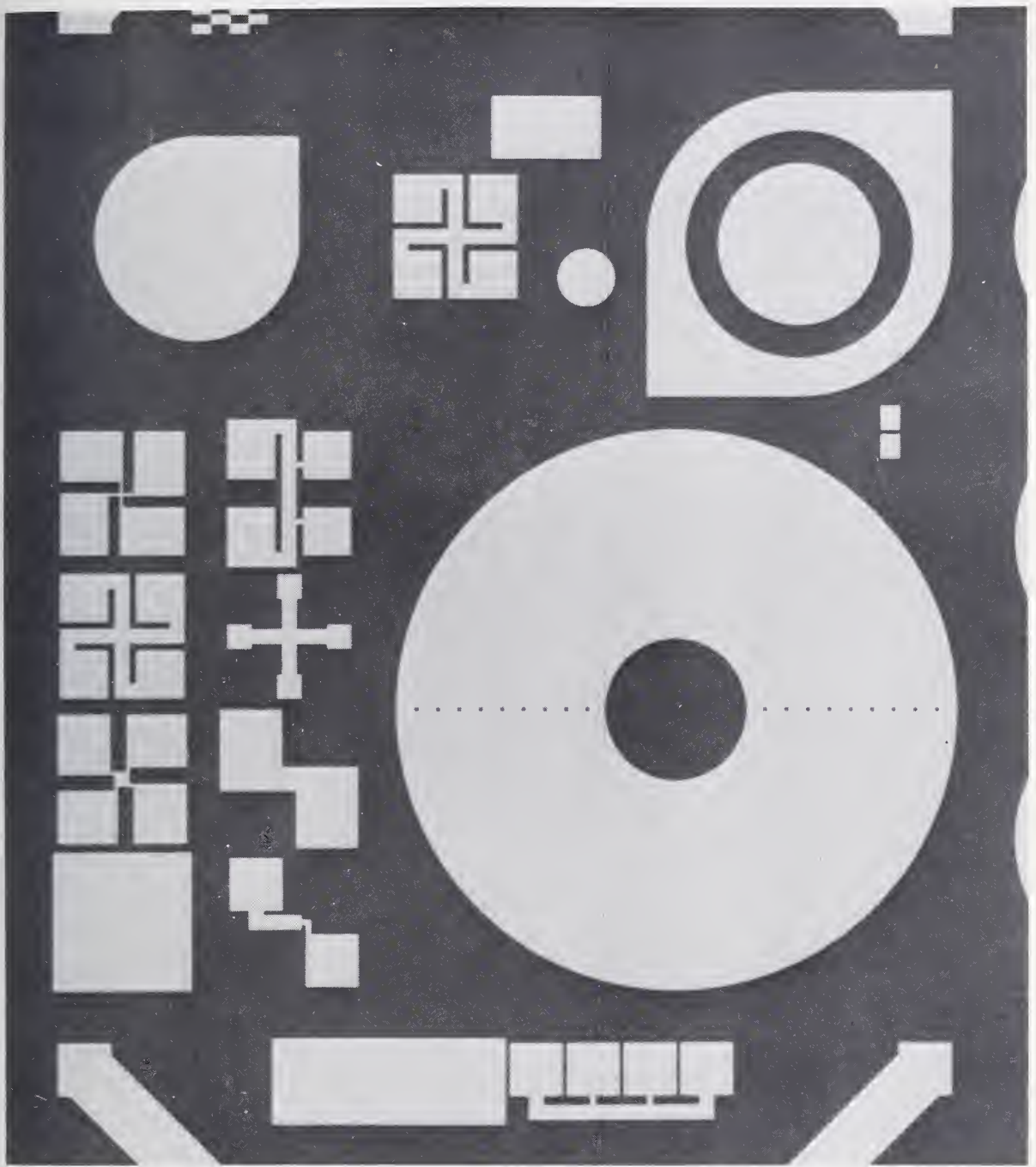


Figure 11. BASE mask for quadrant 2 of test pattern NBS-4. Test structures located in this quadrant are listed in table 3.





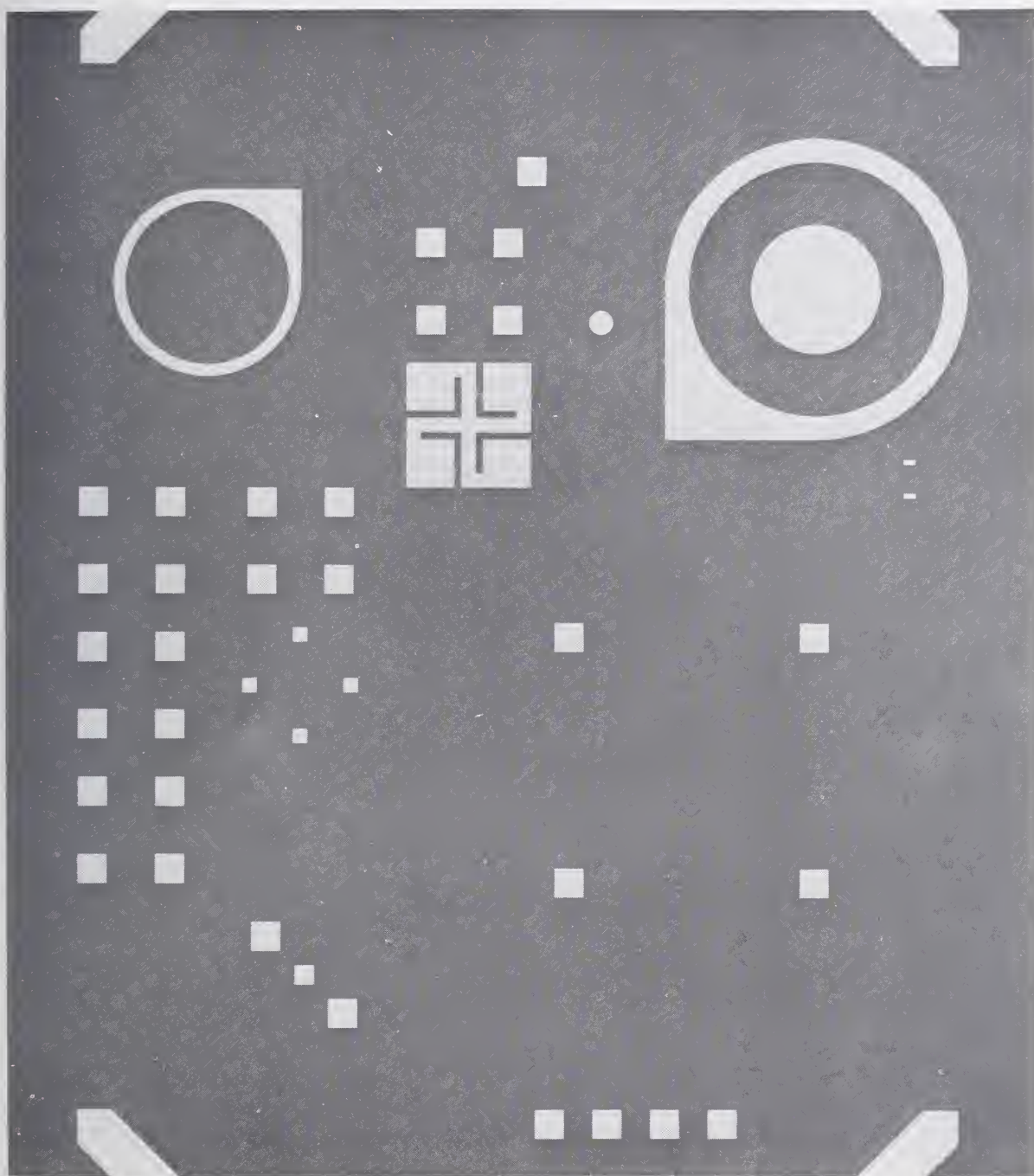


Figure 12. BASE-CONTACT mask for quadrant 2 of test pattern NBS-4. Test structures located in this quadrant are listed in table 3.





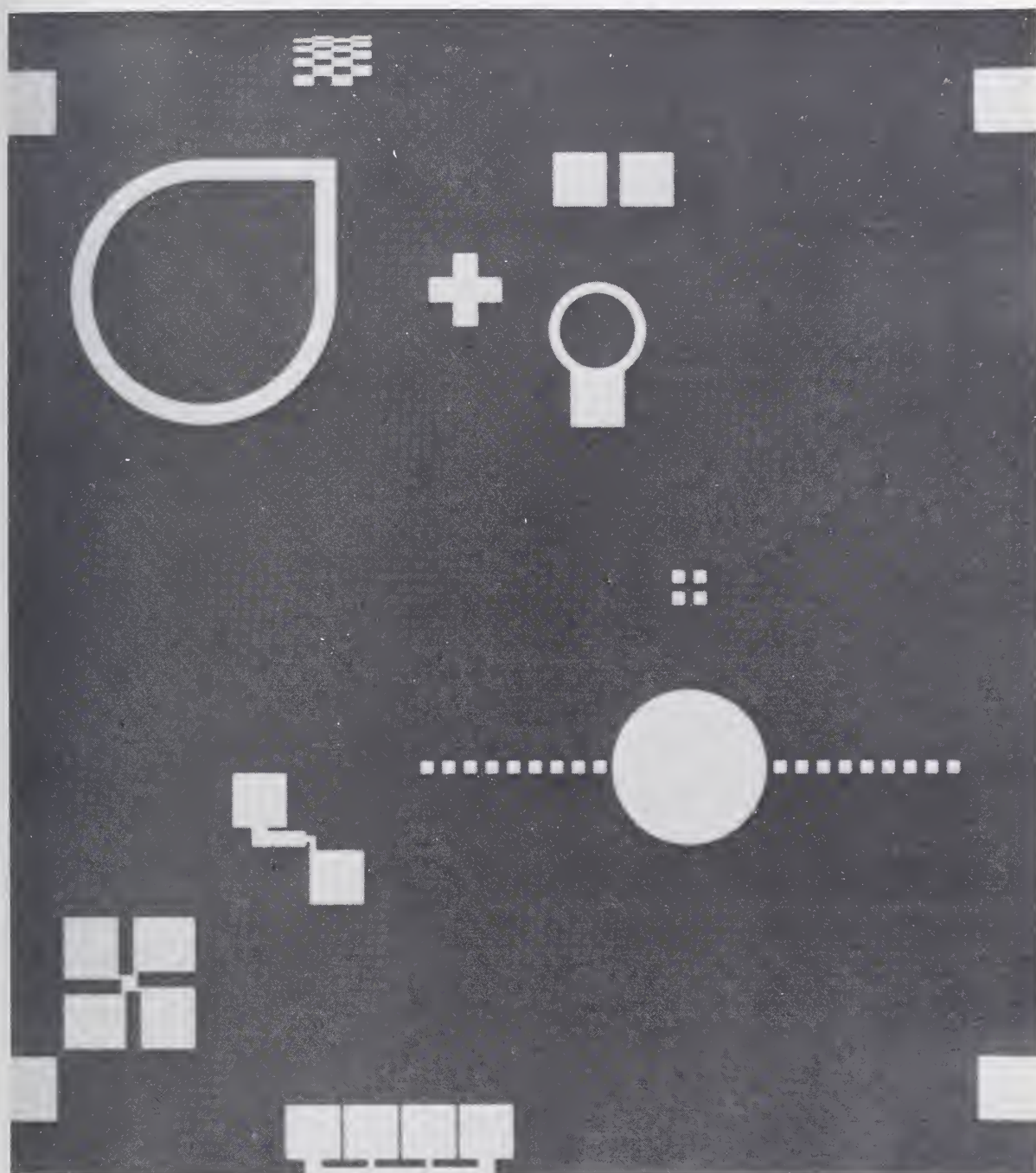


Figure 13. EMITTER mask for quadrant 2 of test pattern NBS-4. Test structures located in this quadrant are listed in table 3.



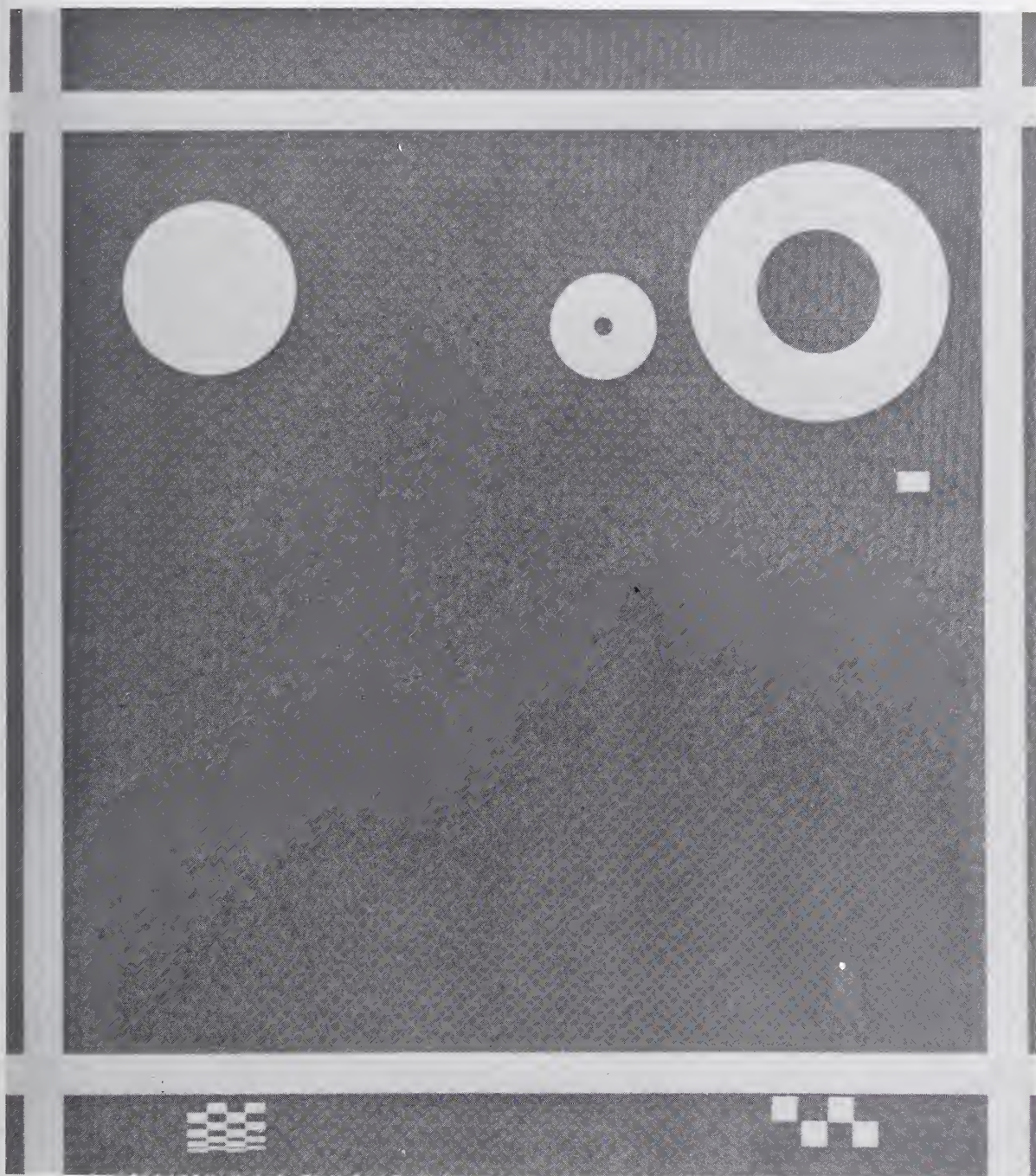


Figure 14. GATE mask for quadrant 2 of test pattern NBS-4. Test structures located in this quadrant are listed in table 3.





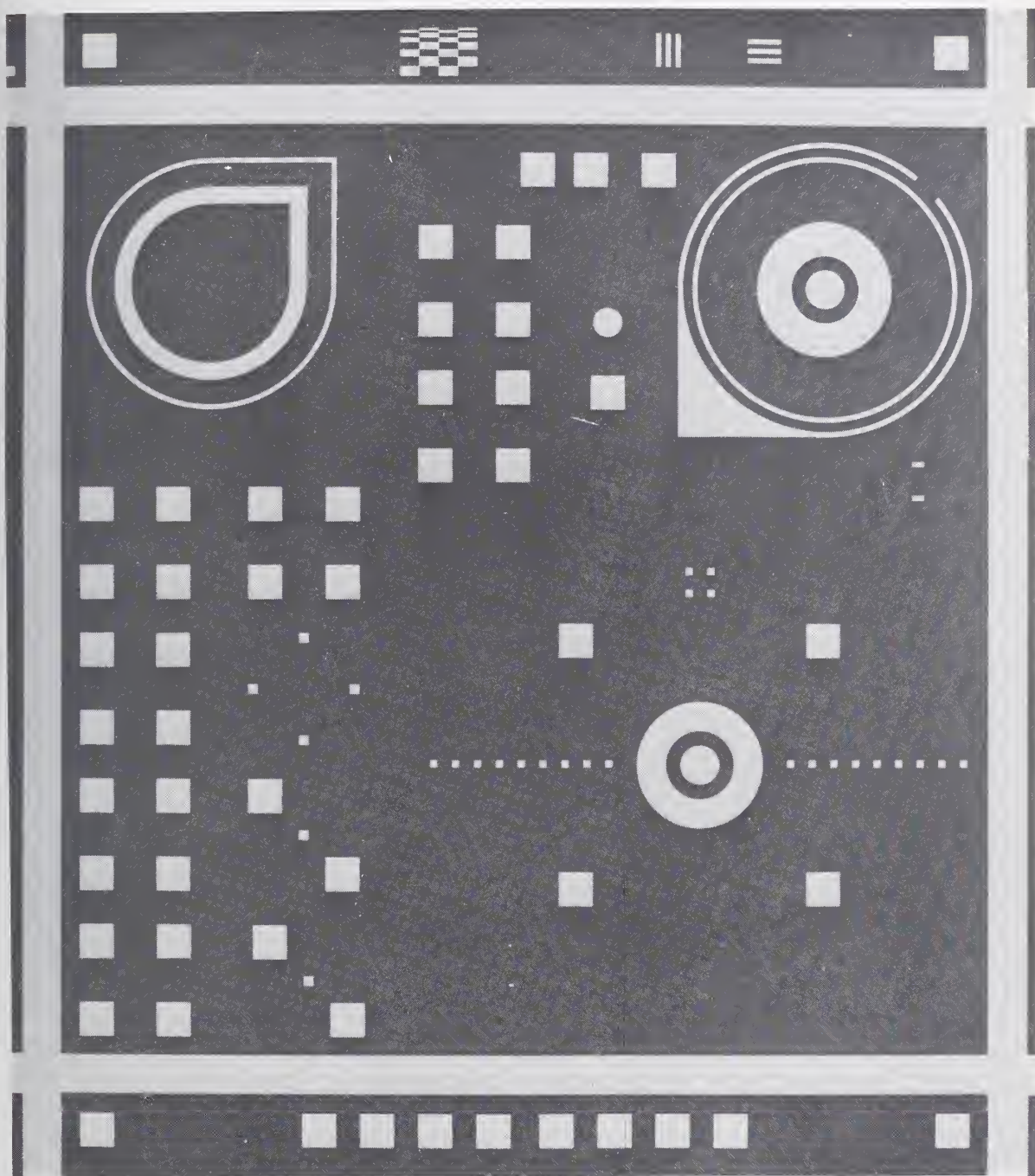


Figure 15. CONTACT mask for quadrant 2 of test pattern NBS-4. Test structures located in this quadrant are listed in table 3.





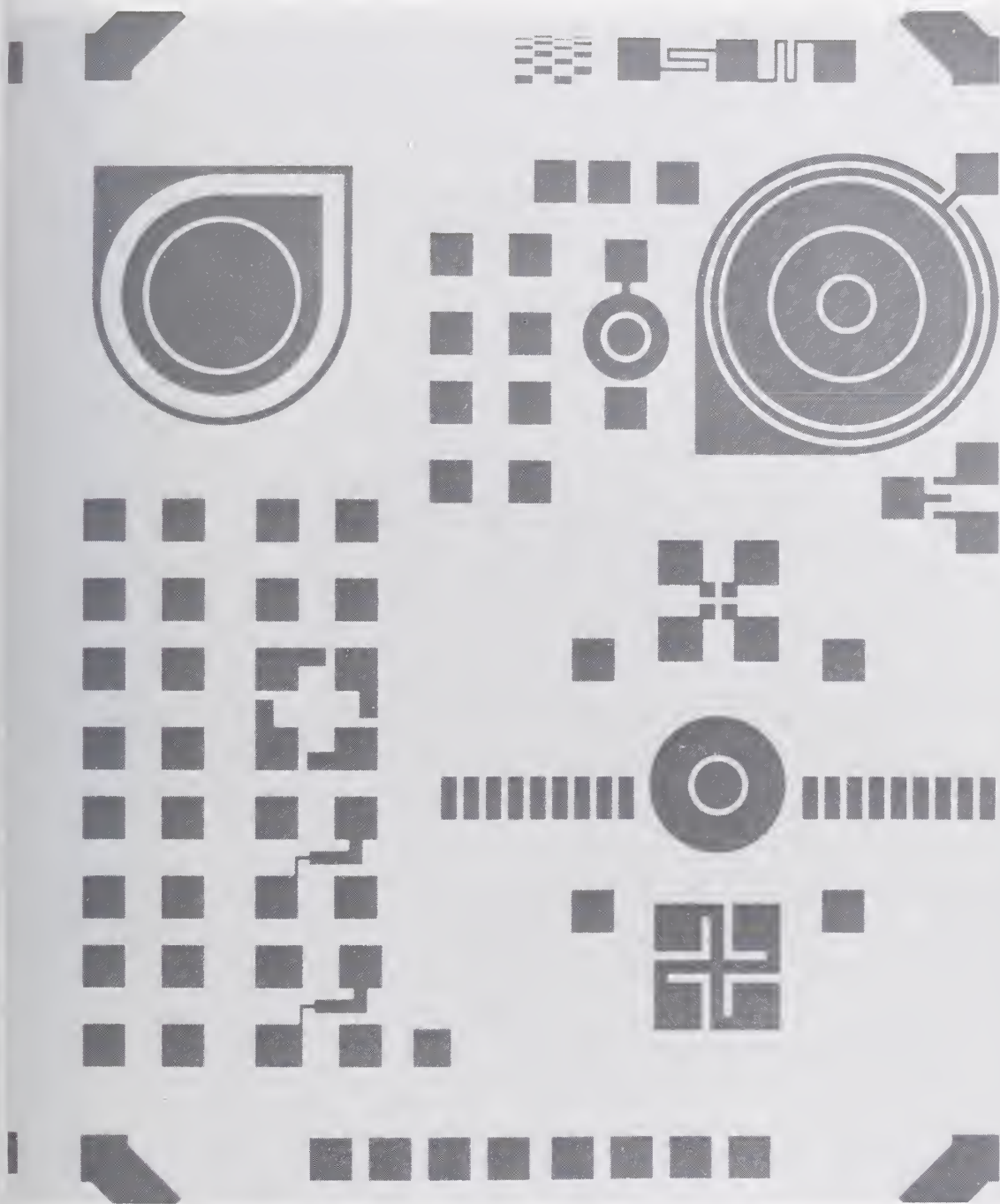


Figure 16. METAL mask for quadrant 2 of test pattern NBS-4. Test structures located in this quadrant are listed in table 3.

Table 4 - Test Structure Shown in Figures 17-23.

Number	Test Structure
4.31	Hall effect device (VDP)

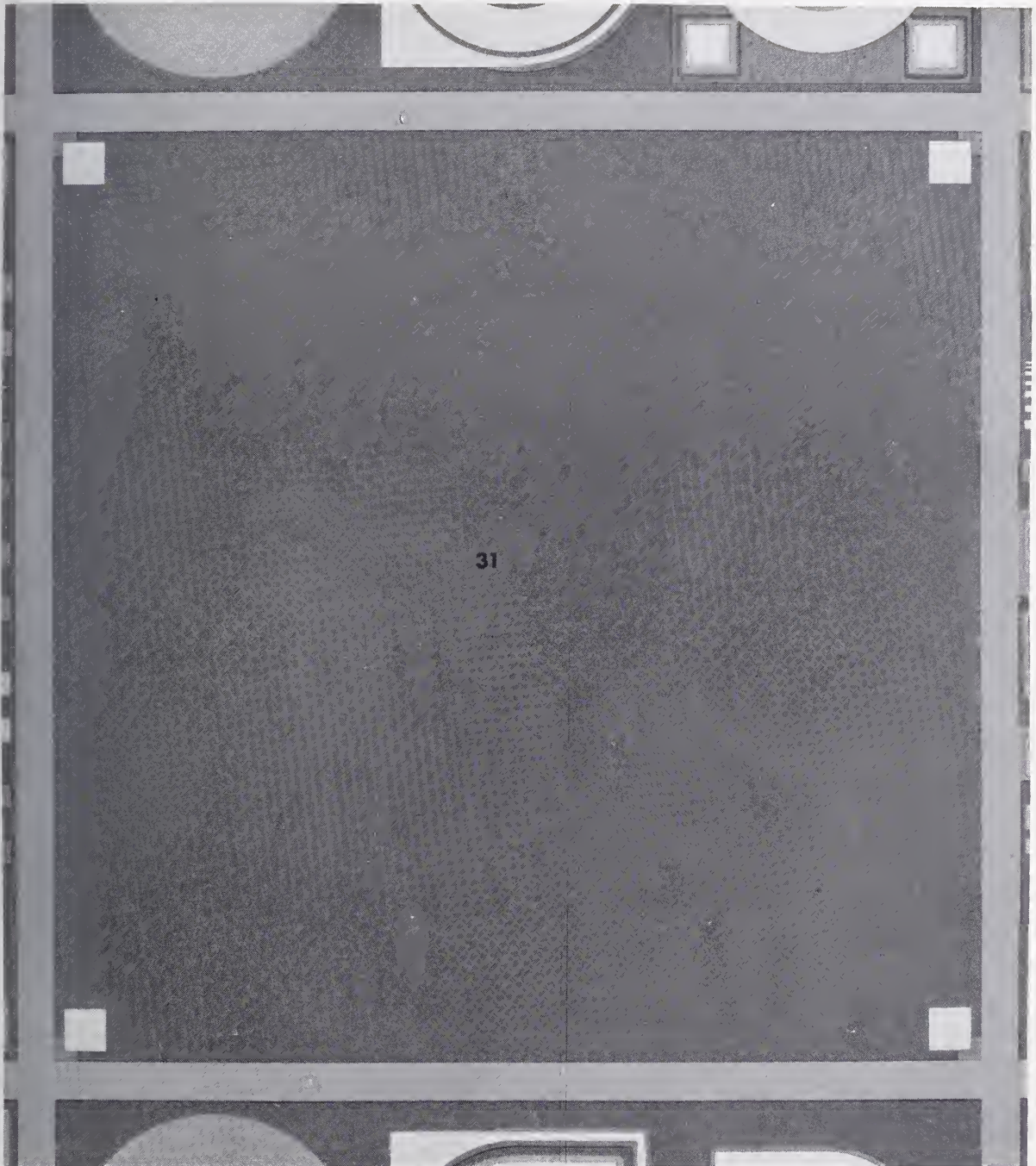


Figure 17. Quadrant 3 of test pattern NBS-4. The only test structure in this quadrant is the Hall effect device listed in table 4.







Figure 18. BASE mask for quadrant 3 of test pattern NBS-4. The Hall effect device is the only test structure located in this quadrant. This figure is included for completeness even though the structure has no base diffusion.





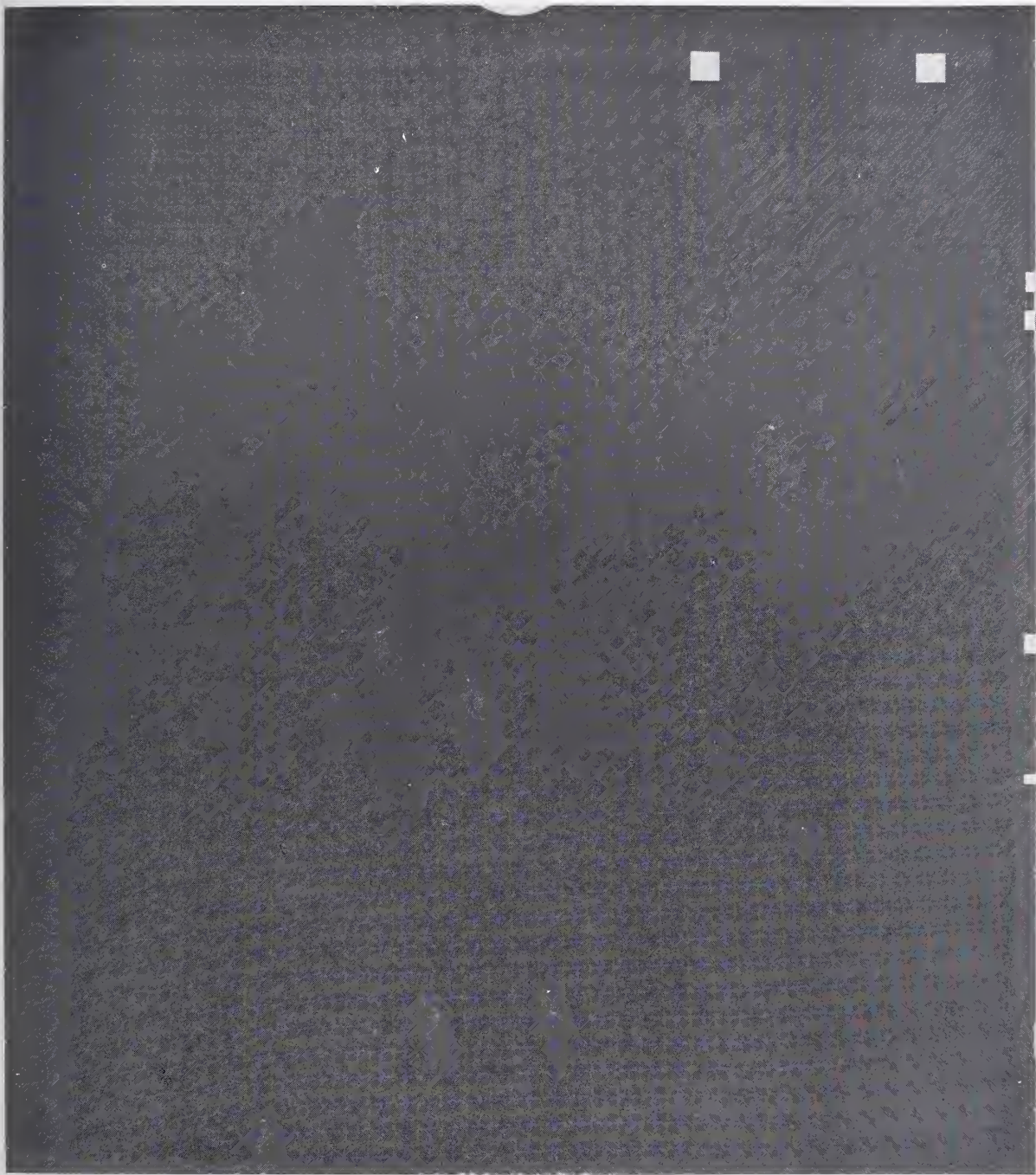


Figure 19. BASE-CONTACT mask for quadrant 3 of test pattern NBS-4. The Hall effect device is the only test structure located in this quadrant. This figure is included for completeness even though the structure has no base contact diffusion.







Figure 20. EMITTER mask for quadrant 3 of test pattern NBS-4. The Hall effect device is the only test structure located in this quadrant.





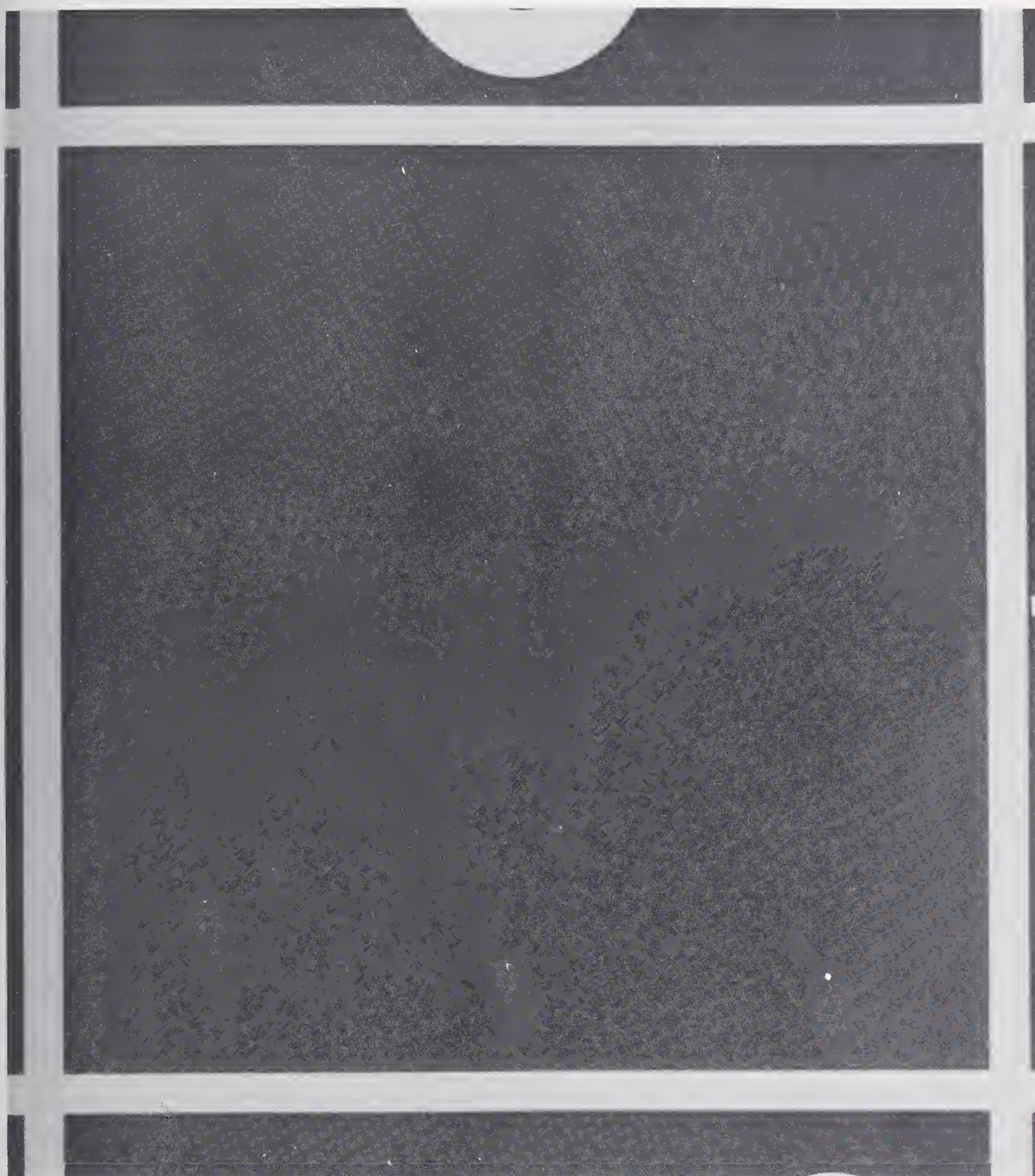


Figure 21. GATE mask for quadrant 3 of test pattern NBS-4. The Hall effect device is the only test structure located in this quadrant. The GATE mask is not involved in the fabrication of this structure, but it does remove oxide from the scribe lines surrounding the structure.





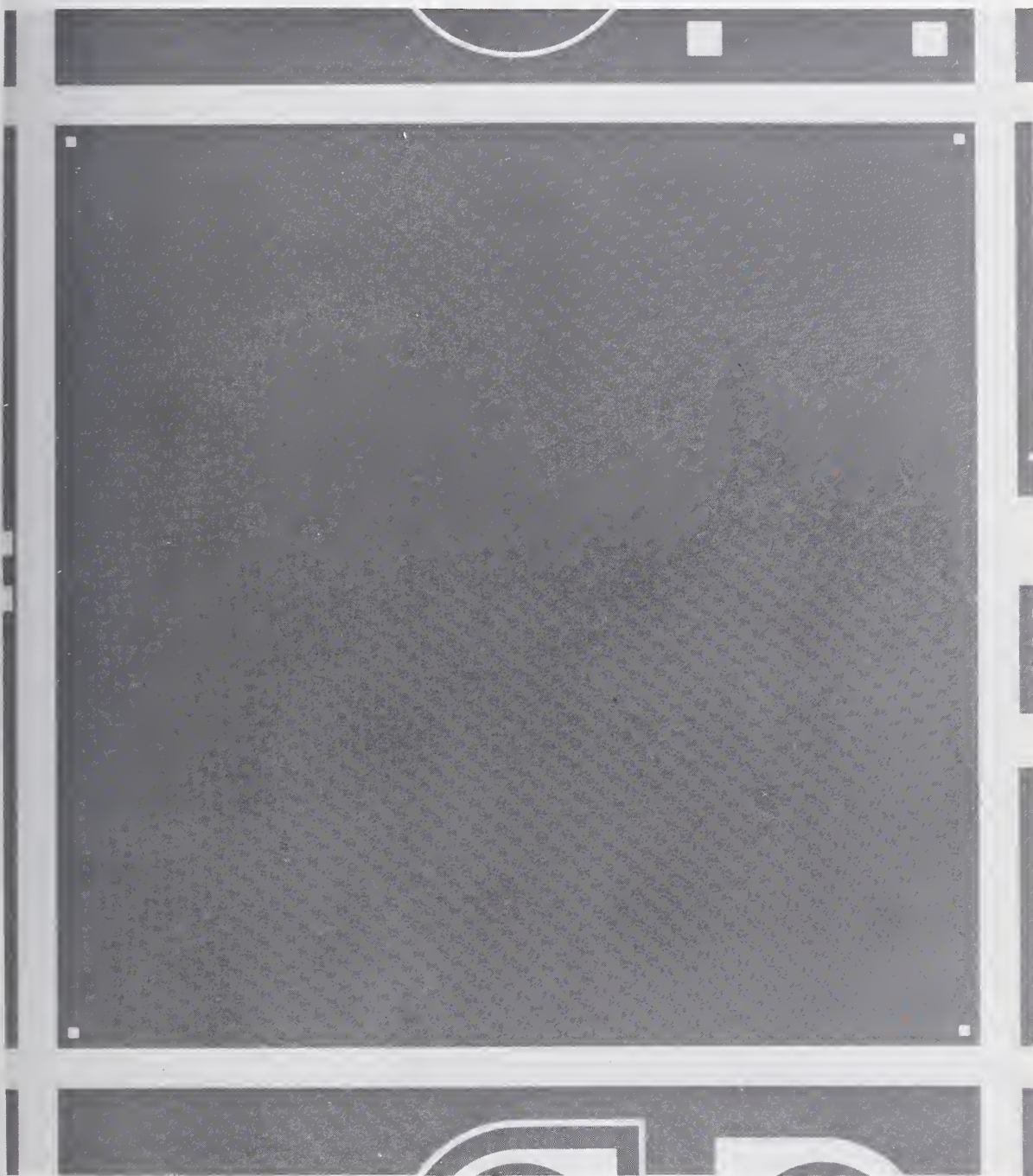


Figure 22. CONTACT mask for quadrant 3 of test pattern NBS-4. The Hall effect device is the only test structure located in this quadrant.





Figure 23. METAL mask for quadrant 3 of test pattern NBS-4. The Hall effect device is the only test structure located in this quadrant.



Table 5 - Test Structures Shown in Figures 24-30.

Number	Test Structure
4.32	Emitter sheet resistor (bridge, $W/L = 0.25$ )
4.33	Base sheet resistor (bridge, $W/L = 0.25$ )
4.34	Surface profilometer structure
4.35	Incremental base sheet resistor (VDP)
4.36	Etch-control structures
4.37	Resolution structures
4.38	Metal step-coverage resistor

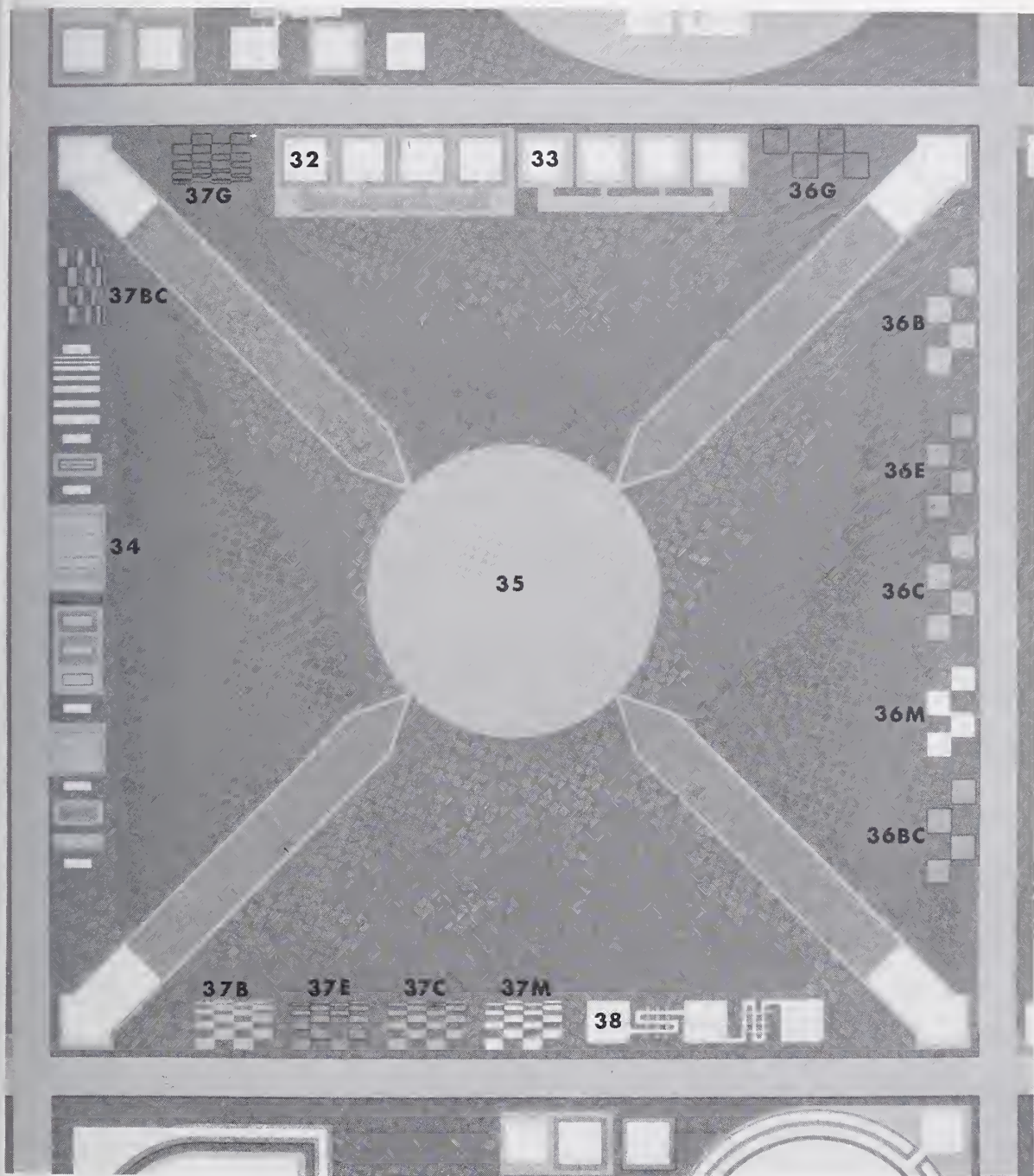


Figure 24. Quadrant 4 of test pattern NBS-4. Test structures are identified in table 5.





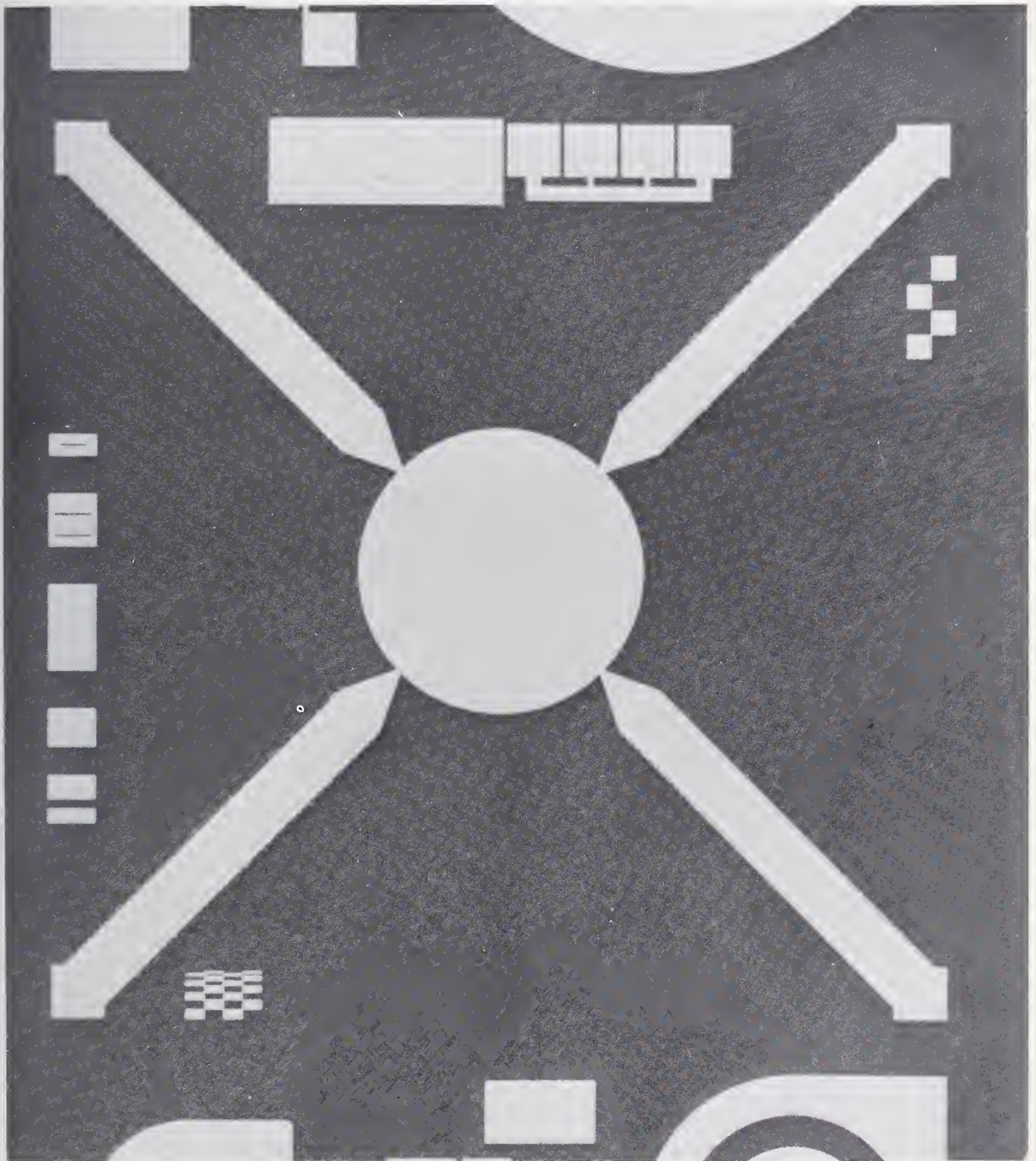


Figure 25. BASE mask for quadrant 4 of test pattern NBS-4. Test structures located in this quadrant are listed in table 5.





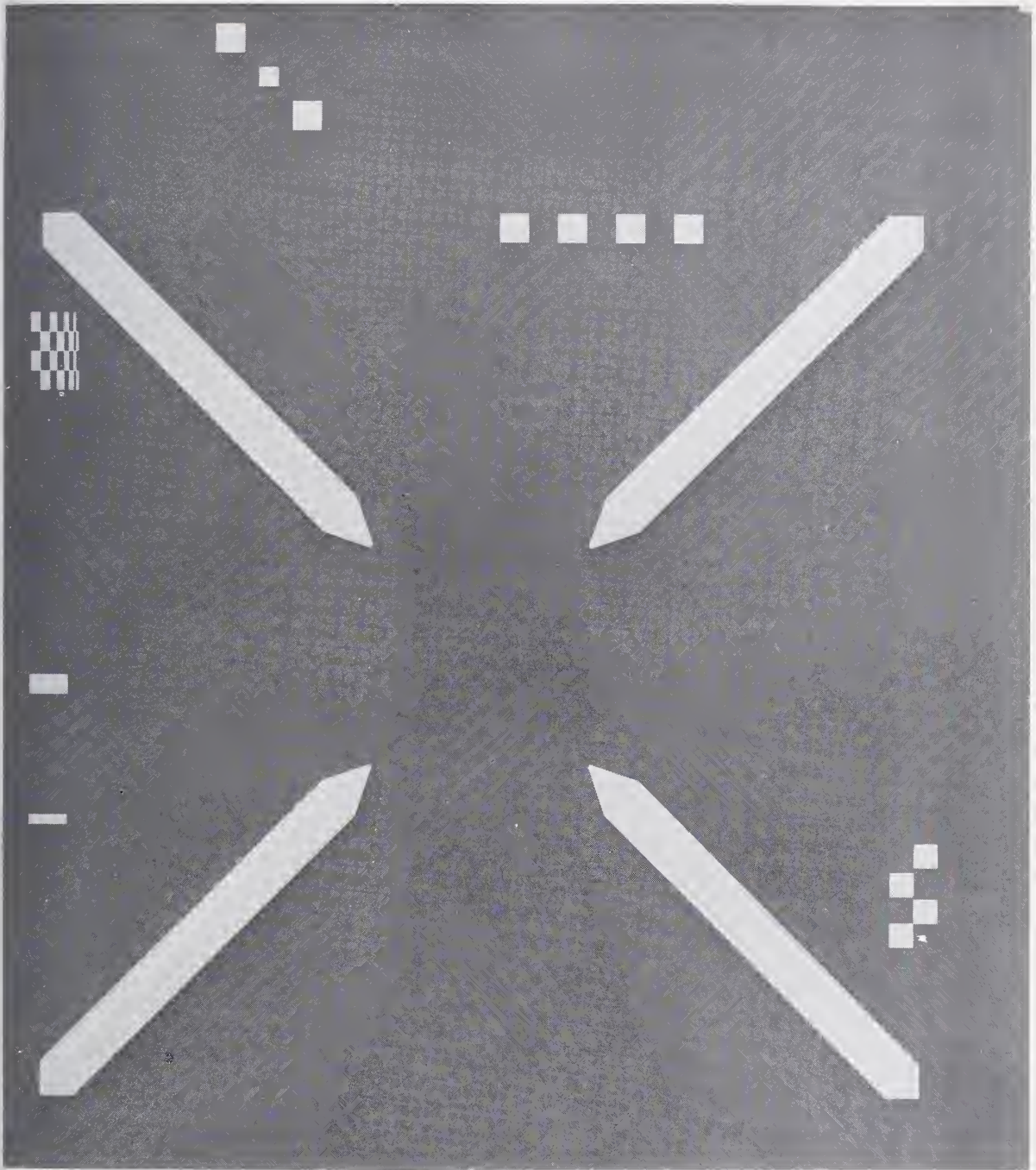


Figure 26. BASE-CONTACT mask for quadrant 4 of test pattern NBS-4. Test structures located in this quadrant are listed in table 5.





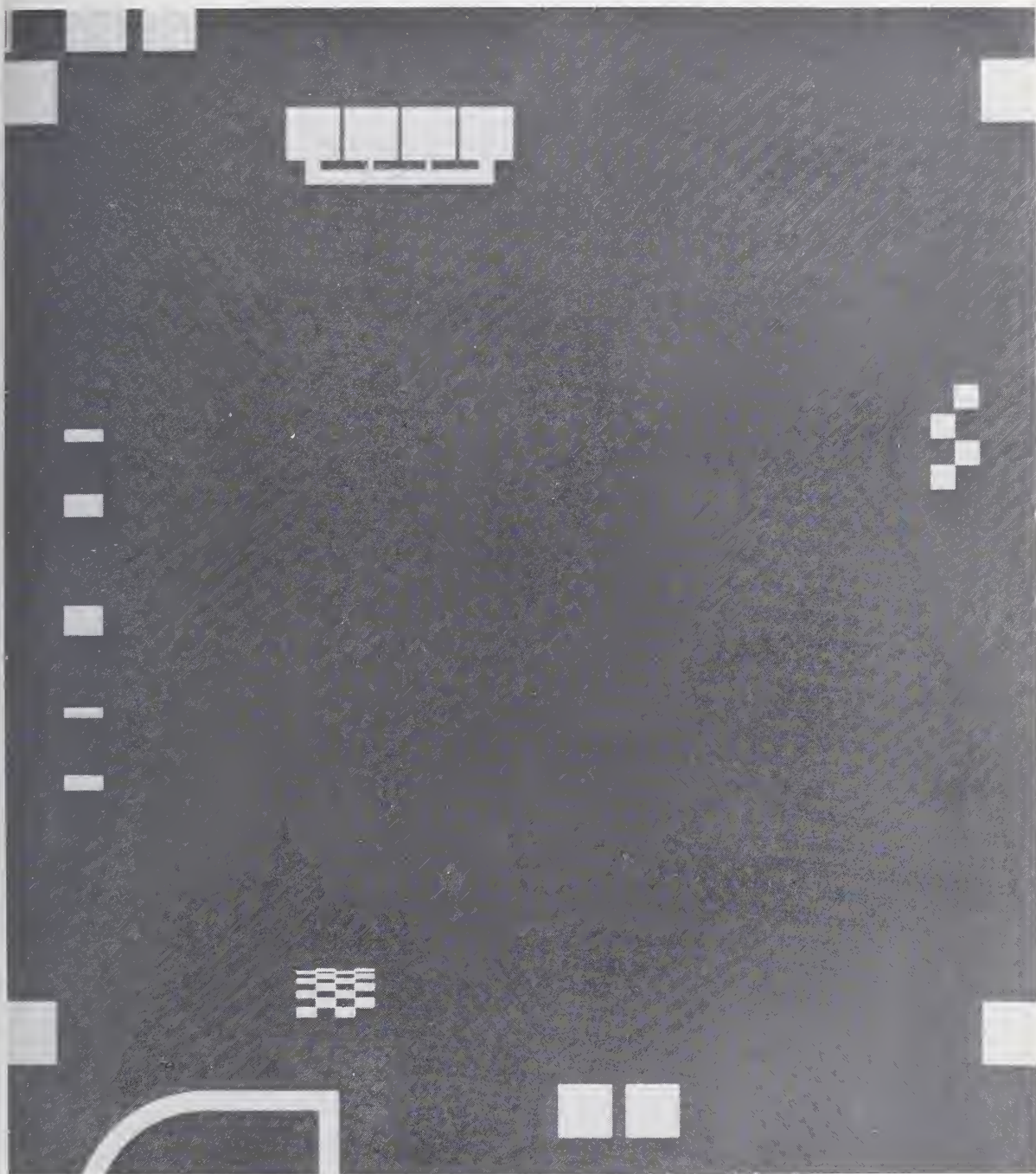


Figure 27. EMITTER mask for quadrant 4 of test pattern NBS-4. Test structures located in this quadrant are listed in table 5.



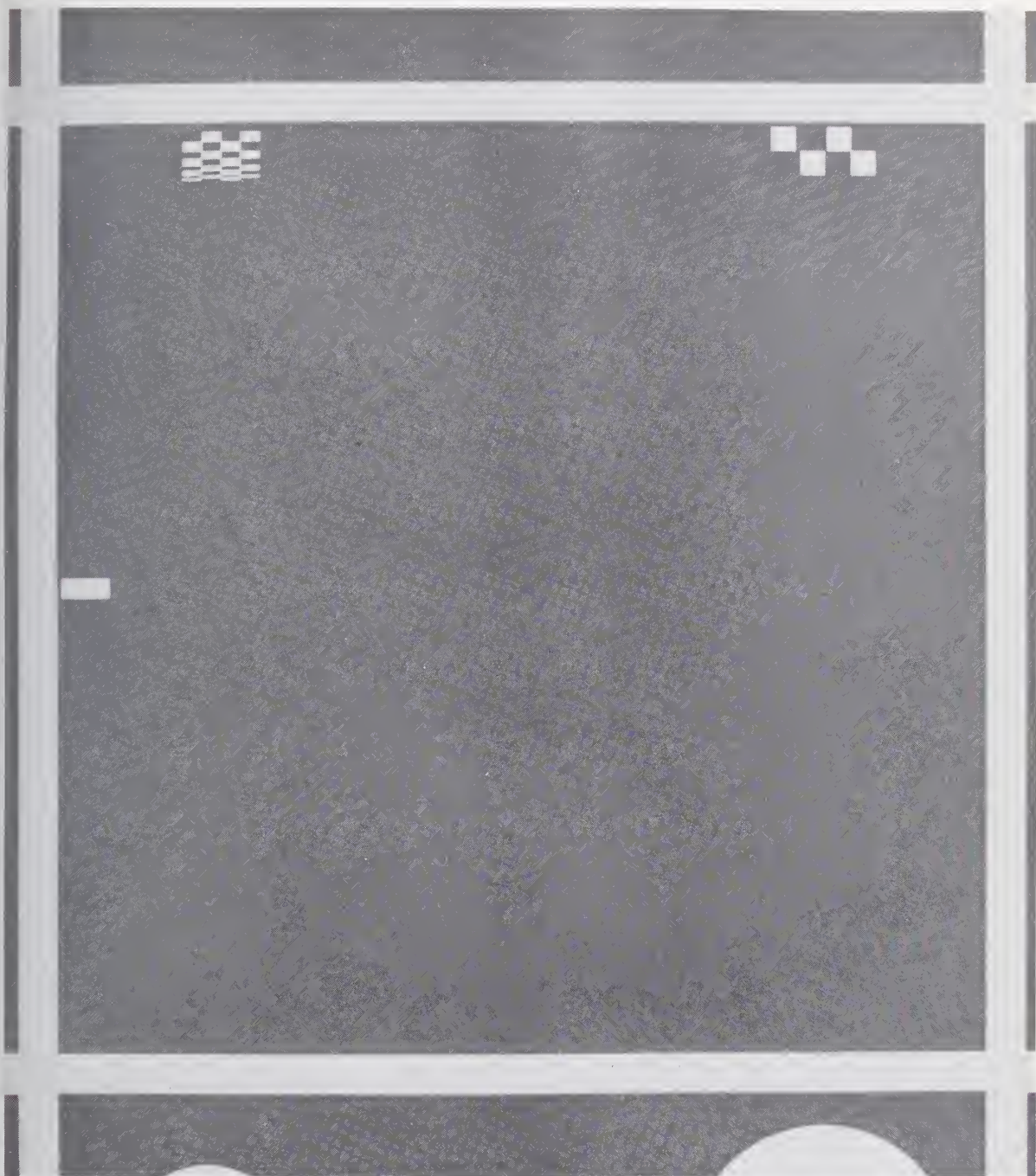


Figure 28. GATE mask for quadrant 4 of test pattern NBS-4. Test structures located in this quadrant are listed in table 5.





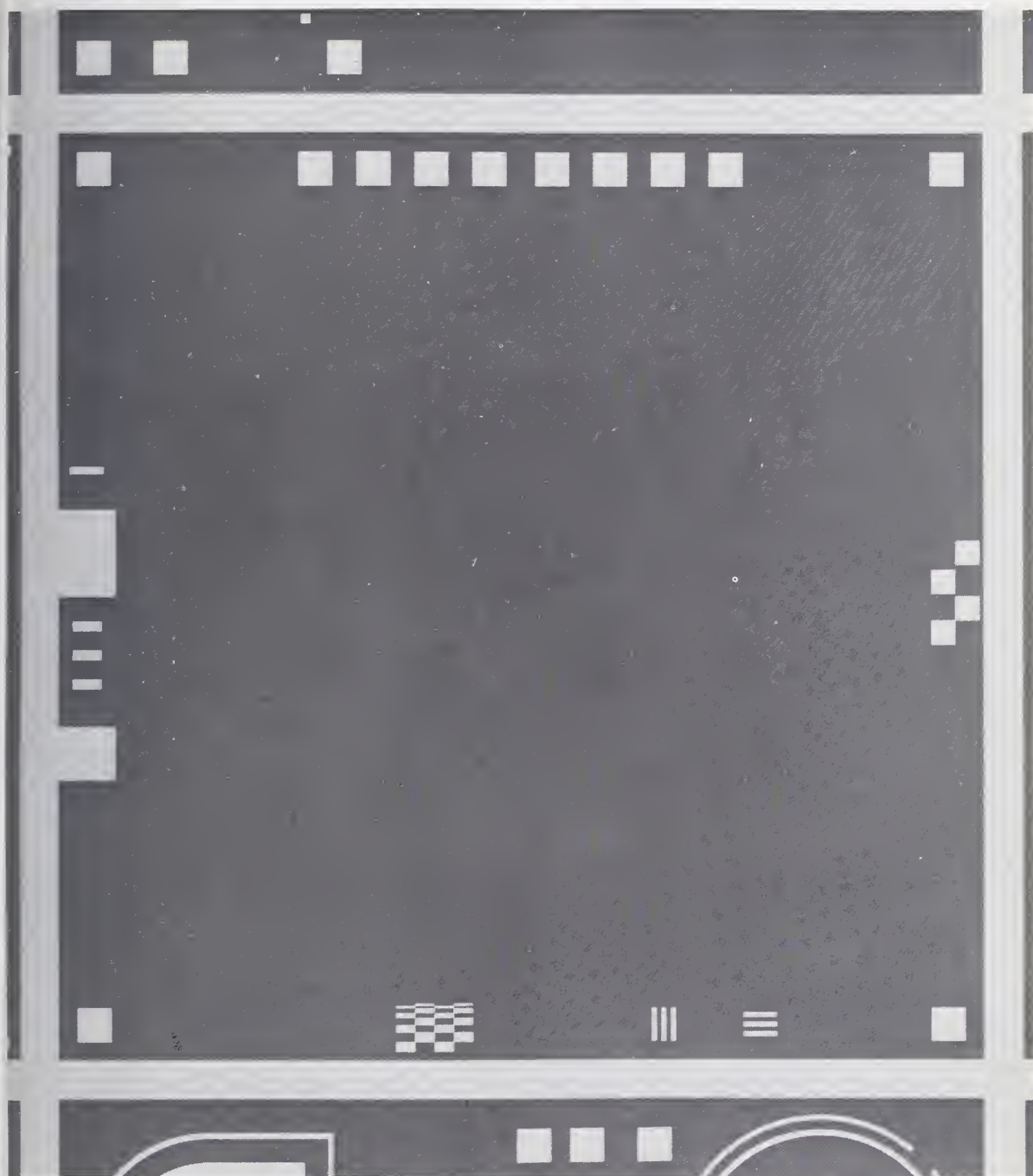


Figure 29. CONTACT mask for quadrant 4 of test pattern NBS-4. Test structures located in this quadrant are listed in table 5.





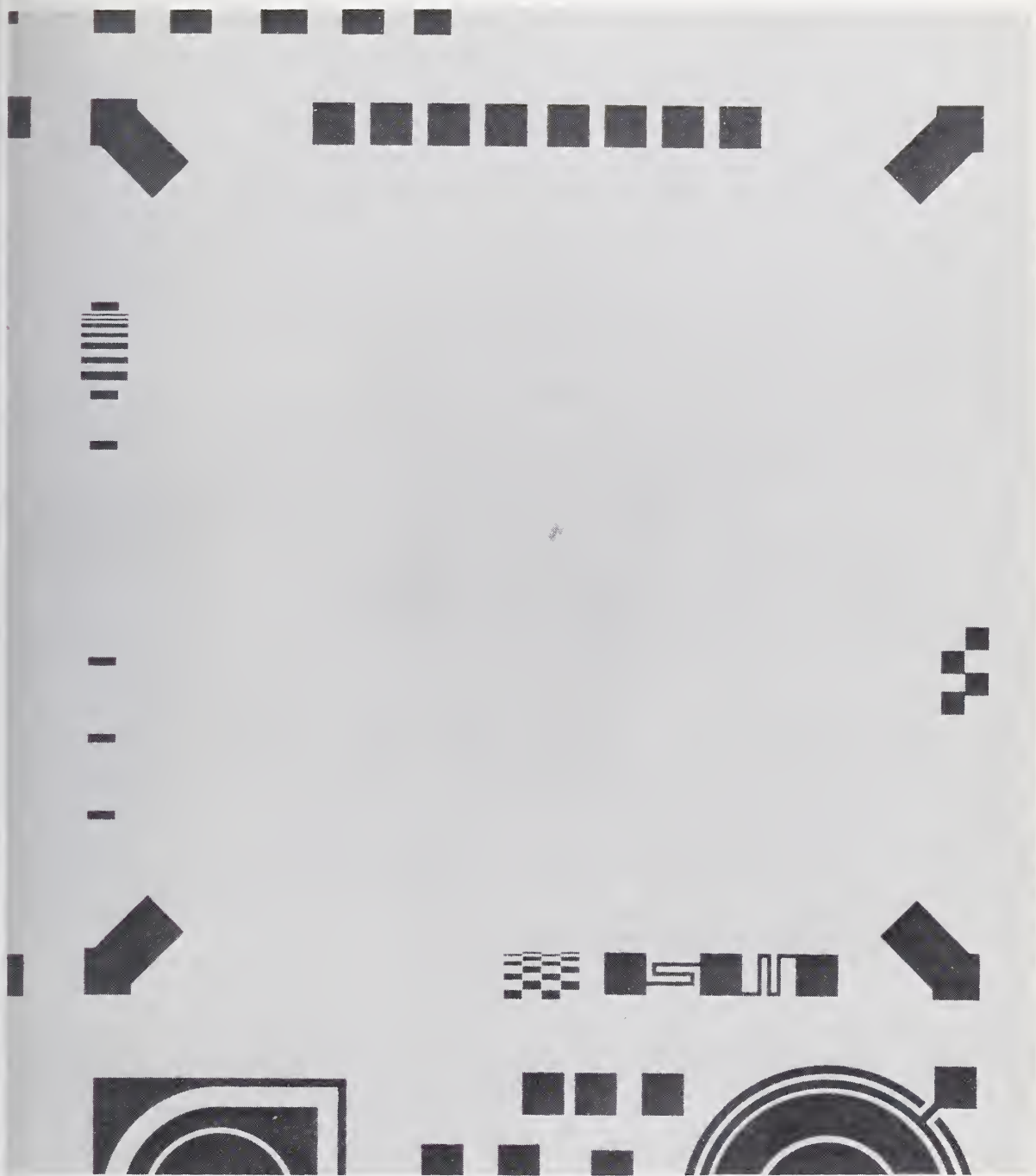


Figure 30. METAL mask for quadrant 4 of test pattern NBS-4. Test structures located in this quadrant are listed in table 5.



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16. ABSTRACT (A 200-word or less factual summary of most significant information. If document includes a significant bibliography or literature survey, mention it here.)  Microelectronic test pattern NBS-4 is a revision of test pattern NBS-3 which was designed primarily for evaluation of the resistivity-dopant density relationship in silicon. Major changes include the addition of optional BASE-CONTACT and GATE masks and the incorporation of several new structures, some useful for the resistivity-dopant density work, and others, mostly sheet resistors, included for evaluation of new designs.  The NBS-4 pattern contains 38 test structures such as planar four-probe resistors, sheet resistors, MOS capacitors, <i>p-n</i> junctions, bipolar and MOS transistors, Hall effect device, and process control structures. The overall pattern is a square 200 mil (5.08 mm) on a side and is divided into four quadrants which are separated by scribe lines. A detailed layout of each structure is presented including both a top view and a cross sectional view. Photomicrographs of each quadrant and the quadrants of the six masks used in the fabrication of the pattern are shown in an appendix.			
17. KEY WORDS (six to twelve entries; alphabetical order; capitalize only the first letter of the first key word unless a proper name; separated by semicolons) Dopant density; microelectronics; MOS capacitors; <i>n-p-n</i> transistor fabrication; <i>p-n</i> junctions; resistivity; semiconductor electronics; sheet resistors; silicon; test pattern; test structures.			
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NOTE: At present the principal publication outlet for these data is the Journal of Physical and Chemical Reference Data (JPCRD) published quarterly for NBS by the American Chemical Society (ACS) and the American Institute of Physics (AIP). Subscriptions, reprints, and supplements available from ACS, 1155 Sixteenth St. N.W., Wash., D.C. 20056.

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